The 17th IEEE International Conference on High Performance Computing and Communications
HPCC 2015
The 12th IEEE International Conference on Embedded Software and Systems
ICESS 2015
The 7th IEEE International Symposium on Cyberspace Safety and Security
CSS 2015

August 24 – 26, 2015
New York, USA

Conference Program and Information Booklet

Organized By
IEEE HPCC/ICESS/CSS 2015 Committees

Sponsored By
IEEE, IEEE TCSC, IEEE Computer Society,
Pace University
## HPCC/ICESS/CSS 2015 Program at a Glance

### Monday, August 24

<table>
<thead>
<tr>
<th>Time</th>
<th>Ball room</th>
<th>Room 1-A</th>
<th>Room 1-B</th>
<th>Room 1-C</th>
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<th>Room 2-A</th>
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<tr>
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<td>HPCC KN-Lu</td>
<td>ICESS 1</td>
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<td>ICESS 3</td>
<td>BigData 1</td>
<td>CSS 4</td>
<td>CSS 5</td>
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<td>10:10</td>
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<td>14:30</td>
<td>ICESS KN-Shukla</td>
<td>HPCC CCC 1</td>
<td>HPCC PEM 1</td>
<td>HPCC BDIA1</td>
<td>HPCC PDC 1</td>
<td>HPCC EES 1</td>
<td>HPCC SEC 1</td>
<td>HPCC OAA 1</td>
<td>HPCC MCCN 1</td>
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<td>HPCC PDC 2</td>
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<td>Smart 1</td>
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<td>18:20</td>
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### Tuesday, August 25

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<td>HPCC CCC 2</td>
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<td>HPCC PDC 3</td>
<td>HPCC PDC 4</td>
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<td>HPCC EST 1</td>
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<td>HPCC EAA 1</td>
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<td>(Short) HPCC ESEC 1</td>
<td>HPCC ESEC 2</td>
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<td>ICESS KN-Wang</td>
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## HPCC/ICESS/CSS 2015 Program at a Glance

### Wednesday, August 26

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Kernel Machine for Visualization and Classification of Big Data

Sun-Yuan Kung
IEEE Fellow, Princeton University, USA

Professor S.Y. Kung received his Ph.D. Degree in Electrical Engineering from Stanford University in 1977. In 1974, he was an Associate Engineer of Amdahl Corporation, Sunnyvale, CA. From 1977 to 1987, he was a Professor of Electrical Engineering-Systems of the University of Southern California, L.A. Since 1987, he has been a Professor of Electrical Engineering at the Princeton University. In addition, he held a Visiting Professorship at the Stanford University (1984); and a Visiting Professorship at the Delft University of Technology (1984); a Toshiba Chair Professorship at the Waseda University, Japan (1984); an Honorary Professorship at the Central China University of Science and Technology (1994); and a Distinguished Chair Professorship at the Hong Kong Polytechnic University since 2001. His research interests include VLSI array processors, system modelling and identification, neural networks, wireless communication, sensor array processing, multimedia signal processing, bioinformatic data mining and biometric authentication.

Big data has many divergent types of sources, from physical (sensor/IoT) to social and cyber (web) types, rendering it messy and, imprecise, and incomplete. The intensive computing need in big data calls for special hardware and software technologies for parallel and/or distributed computing systems, with architectural platform closely coupled with the novel and error-tolerant data mining technologies. This talk will attempt a balanced coverage between the theoretical foundation, algorithmic innovation, and architectural codesign.

Due to its quantitative (volume and velocity) and qualitative (variety) challenges, big data to the users resembles something like “the elephant to the blind men”. It is imperative to enact a major paradigm shift in data mining and learning tools so that information from diversified sources must be integrated together to unravel information hidden in the massive and messy big data, so that, metaphorically speaking, it would let the blind men “see” the elephant. This talk will address yet another vital “V”-paradigm: “Visualization”. Visualization tools are meant to supplement (instead of replace) the domain expertise (e.g. a cardiologist) and provide a big picture to help users formulate critical questions and subsequently postulate heuristic and insightful answers.
Architecture-aware Algorithms and Software for Peta and Exascale Computing

Jack Dongarra
IEEE Fellow and ACM Fellow, University of Tennessee, USA

Jack Dongarra received a Bachelor of Science in Mathematics from Chicago State University in 1972 and a Master of Science in Computer Science from the Illinois Institute of Technology in 1973. He received his Ph.D. in Applied Mathematics from the University of New Mexico in 1980. He worked at the Argonne National Laboratory until 1989, becoming a senior scientist. He now holds an appointment as University Distinguished Professor of Computer Science in the Computer Science Department at the University of Tennessee and holds the title of Distinguished Research Staff in the Computer Science and Mathematics Division at Oak Ridge National Laboratory (ORNL); Turing Fellow at Manchester University; an Adjunct Professor in the Computer Science Department at Rice University; and a Faculty Fellow of the Texas A&M University's Institute for Advanced Study. He is the director of the Innovative Computing Laboratory at the University of Tennessee. He is also the director of the Center for Information Technology Research at the University of Tennessee which coordinates and facilitates IT research efforts at the University.

In this talk, we examine how high performance computing has changed over the last 10-year and look toward the future in terms of trends. These changes have had and will continue to have a major impact on our software. Some of the software and algorithm challenges have already been encountered, such as management of communication and memory hierarchies through a combination of compile--time and run--time techniques, but the increased scale of computation, depth of memory hierarchies, range of latencies, and increased run--time environment variability will make these problems much harder. We will look at five areas of research that will have an importance impact in the development of software and algorithms. We will focus on following themes:

- Redesign of software to fit multicore and hybrid architectures
- Automatically tuned application software
- Exploiting mixed precision for performance
- The importance of fault tolerance
- Communication avoiding algorithms
Combining Process Algebra with Logic Programming – A Calculus for knowledge based Orchestration

Ruqian Lu

Academy of Mathematics and Systems Science (CAS), China

Ruqian Lu is a professor of computer science of the Institute of Mathematics, Academy of Mathematics and Systems Science, at the same time an adjunct professor of Institute of Computing Technology, Chinese Academy of Sciences and Peking University. He is also a fellow of Chinese Academy of Sciences. His research interests include artificial intelligence, knowledge engineering, knowledge based software engineering, formal semantics of programming languages and quantum information processing. He has published more than 180 papers and 10 books. He has won two first class awards from the Chinese Academy of Sciences and a National second class prize from the Ministry of Science and Technology. He has also won the 2003 Hua Loo-keng Mathematics Prize from the Chinese Mathematics Society and the 2014 lifetime achievements award from the China’s Computer Federation.

This talk presents Knorc – a calculus for KNOWledge based ORChestration, which is a conservative extension of the Orc calculus. Orc is, as claimed by its authors, a language for wide area computation and has been developed at University of Dallas. It is simple and powerful with site calls as program units and four combinators to compose them. There was quite a lot of following up works alone this line. Knorc is yet another extension of Orc in direction of knowledge processing. The main new ingredient is logic programming whose combination with process algebra is a major technical challenge to the design of Knorc. Besides introducing new possibilities of implementing site calls, the advantages of this combination include better structuredness of programs, separation of knowledge content from control flow and reusability of knowledge. The second main ingredient is the availability of a set of different parallel programming paradigms, which makes Knorc a process algebra not only with logic programming facilities, but also with powerful parallel logic programming facilities. In particular, it is possible to do massive parallel programming in Knorc. The third main ingredient is the introduction of a specific data type – the abstract knowledge sources to increase its knowledge processing power. While Orc has no data types at all, several extension works in the literature have introduced different data types, e.g. the XML data type. The introduction of abstract knowledge sources makes Knorc a language based on Open World Assumption, rather than Closed World Assumption. We have formalized the syntax and semantics of Knorc. A first implementation of Knorc is underway.
Exploiting Hierarchical Locality for Productive Extreme Computing

Tarek El-Ghazawi
Professor and IEEE Fellow, The George Washington University

Tarek El-Ghazawi is a Professor in the Department of Electrical and Computer Engineering at The George Washington University, where he leads the university-wide Strategic Academic Program in High-Performance Computing. His research interests include high-performance computing, computer architecture, reconfigurable computing and parallel programming. He is the founding director of The GW Institute for Massively Parallel Applications and Computing Technologies (IMPACT) and a founding Co-Director of the NSF Industry/University Center for High-Performance Reconfigurable Computing (CHREC). He is one of the principal co-authors of the UPC parallel programming language and the primary author of the UPC book from John Wiley and Sons. He has received his Ph.D. degree in Electrical and Computer Engineering from New Mexico State University in 1988. El-Ghazawi has published well over 250 refereed research publications in this area. Dr. El-Ghazawi has served in many editorial roles including an Associate Editor for the IEEE Transactions on Computers. He chaired and co-chaired many international conferences and symposia. He has served on many advisory boards and in consulting roles including service as a consultant at NASA GSFC and NASA Ames.

Modern high-performance computers are characterized with massive hardware parallelism and deep hierarchies. Hierarchical levels may include cores, dies, chips, and nodes to name a few. Locality exploitation at all levels of the hierarchy is a must as the cost of data transfers can be high. Programmer’s knowledge and the expressivity of locality-aware programming models such as the Partitioned Global Address Space (PGAS) can be very useful. However, locality awareness can come at a high cost. In addition, asking programmers to worry about expressing locality relations at multiple architecture hierarchy levels is detrimental to productivity and systems and hardware must provide adequate support for exploiting hierarchical locality.

In this talk I will discuss a framework for understanding and exploiting hierarchical locality in preparation for the next era of extreme computing. The role of system and hardware support will be highlighted will be stressed and examples will be shared.
Smart-Grid: Where Embedded Computing, Communication and Power Systems Meet

Sandeep K Shukla
Indian Institute of Technology Kanpur

Professor Sandeep K. Shukla received his bachelor’s degree in Computer Science and Engineering at Jadavpur University, Kolkata in 1991, his Masters and PhD degrees in Computer Science from the State University of New York at Albany, NY, USA in 1995 and 1997 respectively. He worked as a scientist at the GTE labs on telecommunications network management, distributed object technology, and event correlation technologies 1997-1999. Between 1999 and 2001, he worked at the Intel Corporation on the formal verification of the ITANIUM processor, and on system level design languages. 2001-2002, he was a research faculty at the University of California at Irvine working on embedded system design. He received the prestigious Presidential Early Career Award for Scientists and Engineers (PECASE) from the White House in 2004, Frederich Wilhelm Bessel Award in 2008 from the Humboldt Foundation, Germany, ACM Distinguished Scientist in 2013, and IEEE Fellow in 2014. He also served as ACM Distinguished Speaker between 2007 and 2015, IEEE Computer Society Distinguished Visitor between 2008 and 2012.

The vision of a smart grid is predicated upon pervasive use of embedded intelligence, and digital communication techniques in today's power system. As wide area measurements and control techniques are being developed and deployed for a more resilient power system, the role of computing and communication network is becoming inalienable. The system state estimation, protection, control of oscillations are real-time computing applications. Similarly, the power system dynamics gets influenced by the communication delays in the network. Therefore, extensive integration of power system and its computing/communication infrastructure mandates that the two systems are studied as a single distributed cyber-physical system. In this talk we will discuss some of the problems and their solutions germane to this inter-dependency between two critical infrastructures. In particular, a power/network co-simulation framework which integrates power system dynamic simulator and network simulator together using an accurate synchronization mechanism will be discussed. The accuracy of this co-simulation system is tunable based on the time-scale requirements of the phenomena being studied. This co-simulation can improve the practical investigation of smart grid and evaluate wide area measurement and control schemes. We will also discuss some case studies including an agent-based remote backup relay system simulated and validated on this co-simulation framework.
Event-driven Decentralized Statistical Signal Processing

Xiaodong Wang
Professor, Columbia University, USA

Xiaodong Wang was an assistant professor from July 1998 to December 2001 at the Department of Electrical Engineering at Texas A&M University. In January 2002, he joined the Department of Electrical Engineering at Columbia University as an assistant professor. Dr. Wang's research interests fall in the general areas of computing, signal processing, and communications. He has worked and published extensively in the areas of wireless communications, statistical signal processing, parallel and distributed computing, nanoelectronics, and quantum computing. Dr. Wang has received the 1999 NSF CAREER Award. He has also received the 2001 IEEE Communications Society and Information Theory Society Joint Paper Award.

For many emerging applications that rely on scarce energy resources (e.g., wireless sensor networks), event-driven sampling, in which a sample is taken when a significant event occurs in the signal, is a promising alternative to the conventional uniform sampling. In these event-based sampling methods, samples are taken based on the signal amplitude instead of time, as opposed to the conventional uniform sampling. As a result, the signal is encoded in the sampling times, whereas in uniform sampling the sample amplitudes encode the signal. This yields a significant advantage in real-time applications, in which sampling times can be tracked via simple one-bit signaling. In this talk, we present the use of event-driven sampling as a means of information transmission for decentralized detection and estimation. We start with the decentralized detection problem where we address the challenge of noisy transmission channels via level-triggered sampling. Then, we discuss the sequential estimation of linear regression parameters under a decentralized setup. Using a variant of level-triggered sampling we design a decentralized estimator that achieves a close-to-optimum average stopping time performance, and linearly scales with the number of parameters while satisfying stringent energy and computation constraints. Finally, we discuss decentralized sequential joint detection and estimation. Applications in cognitive radio and smart grid will be presented.
IEEE International Conference on High Performance Computing and Communications (HPCC 2015)

HPCC CCC 1: Cloud and Cluster Computing
Monday 14:30, Room 1-A  Session Chair: Yongxin Zhu
Availability-Aware Virtual Network Embedding for Multi-Tier Applications in Cloud Networks
Meng Shen, Xu Ke, Fuliang Li, Fan Li, Liehuang Zhu and Lei Guan

AzureRender: A Cloud-Based Parallel and Distributed Rendering System
Zhenbang Liu and Hengming Zou

CPPStreaming: a Cloud-assisted Peer-to-Peer Live Streaming System
Laizhong Cui, Genghui Li, Xianghua Fu and Nan Lu

Yang Sun, Mengshi Hu, Bin Wang, Yongyu Chang and Dacheng Yang

HPCC CCC 2: Cloud and Cluster Computing
Tuesday 08:30, Room 1-A  Session Chair: Jun-Jie Peng
Modeling for CPU-intensive Applications in Cloud Computing
Jun-Jie Peng

Nutshell: Cloud Simulation and Current Trends
Ubaid Rehman, Kashif Bilal, Laurence Yang and Samee Khan

Performance Evaluation of Energy-aware Best Fit Decreasing Algorithms for Cloud Environments
Saad Mustafa, Kashif Bilal, Samee Khan and Laurence Yang

A Cost and Contention Conscious Scheduling for Recovery in Cloud Environment
Pham Phuoc Hung and Tuan-Anh Bui

HPCC CCC 3: Cloud and Cluster Computing
Tuesday 13:30, Room 1-A  Session Chair: Wenyun Dai
RaHeC: A Mechanism of Resource Management for Heterogeneous Clouds
Wenyun Dai, Haopeng Chen and Wenting Wang

A Head Record Cache Structure to Improve the Operations on Big Files in Cloud Storage Servers
Hongjun Dai

Critical Node Detection Problem Solving on GPU and in the Cloud
Cholpon Degenbaeva and Matthias Klusch
Predicting Scheduling Failures in the Cloud: A Case Study with Google Clusters and Hadoop on Amazon EMR
Mbarka Soualhia, Foutse Khomh and Sofiene Tahar

Customer Churn Aware Resource Allocation and Virtual Machine Placement in Cloud
Qiyuan Yang, Xiaoyu Li and Suman Kumar

HPCC PEM 1: Performance Evaluation and Measurement
Monday 14:30, Room 1-B
Session Chair: Peng Zhang

Performance and Power Analysis of High-Density Multi-GPGPU Architectures: A Preliminary Case Study
Yuxiang Gao, Saeed Iqbal, Peng Zhang and Meikang Qiu

Rethinking Prefetching in GPGPUs: Exploiting Unique Opportunities
Ahmad Lashgar and Amirali Baniasadi

Agent-based High-Performance Simulation of Biological Systems on the GPU
Mark Burkitt, Mariam Kiran, Savas Konur, Marian Gheorghe and Florentine Ipate

HPCC BDIA 1: Big Data Infrastructure and Applications
Monday 14:30, Room 1-C
Session Chair: Laurence Tianruo Yang

Efficiently Trigger Data Races through Speculative Execution
Zhendong Wu, Kai Lu and Xiaoping Wang

Node scaling scheduling of real-time tasks in a power-aware datacenter
Fei Teng, Lei Yu and Tianrui Li

MDDM-A Method to Improve multiple dimension data management performance in HBase
Zhuang Wei, Qu Junmei, Liu Liang, Zhu Chaoqiang and Yin Wenjun

RALD: Reliable Transactional Software Controller for Redundancy Array of Log Structured Disks
Zhenyuan Sun, Mingyang Guo, Huanqing Dong, Zhenjun Liu, Lu Xu and Yunqiu Liu

HPCC BDIA 2: Big Data Infrastructure and Applications
Tuesday 17:00, Room 1-C
Session Chair: Ruixuan Li

An Efficient Data Selection Policy for Search Engine Cache Management
Xinhua Dong, Ruixuan Li, Heng He, Xiwu Gu, Mudar Sarem, Meikang Qiu and Keqin Li

Exploiting Spatial Smoothness in HPC Applications to Detect Silent Data Corruption
Leonardo Arturo Bautista Gomez and Franck Cappello

Maximizing Data Credibility Under Budget Constraint for Participatory Sensing
Hui Gao, Chi Harold Liu, Wendong Wang, Zhengguo Sheng, Alvin Chin and Ye Tian

Hybrid Storage Throughput Allocation Among Multiple Clients in Heterogeneous Data Center
Huo Zhisheng, Xiao Limin, Zhong Qiaoling, Li Shupan, Li Ang, Ruan Li, Wang Shouxin and Fu Lihong
HPCC PDC 1: Parallel and Distributed Computing
Monday 14:30, Room 1-D  Session Chair: Yongxin Zhu

VarFS: a Variable-sized Objects based Distributed File System
Yili Gong, Yanyan Xu, Yingchun Lei and Wenjie Wang

Distributed Discord Discovery: Spark Based Anomaly Detection in Time Series
Yafei Wu, Yongxin Zhu and Tian Huang

WHOBBBS: An Object-based Distributed Hybrid Storage Providing Block Storage for Virtual Machines Storage
Lingxuan Shen, Haopeng Chen, Sixiang Ma, Zhenwei Du and Fei Hu

Performance Prediction for Apache Spark Platform
Kewen Wang and Mohammad Maili Hasan Khan

HPCC PDC 2: Parallel and Distributed Computing
Monday 16:40, Room 1-D  Session Chair: Youtao Zhang

Contention-Free Fair Queuing for High-Speed Storage with RAID-0 Architecture
Myung Hyun Jo and Won Woo Ro

Delay Performance of Direct Reads in Distributed Storage Systems with Coding
Qiqi Shuai and Victor Li

SAUD: Semantics-Aware and Utility-Driven Deduplication Framework for Primary Storage
Yan Tang, Jianwei Yin and Wei Luo

GA based Placement Optimization for Hybrid Distributed Storage
Yizhi Wu and Youtao Zhang

HPCC PDC 3: Parallel and Distributed Computing
Tuesday 08:30, Room 1-C  Session Chair: Bo Li

Research of Massive Small Files Reading Optimization Based on Parallel Network File System
Yang Hongzhang, Zhang Junwei, Zeng Xiangchao, Dong Huanqing and Xu Lu

Optimal Performance Prediction of ADAS Algorithms on Embedded Parallel Architectures
Romain Saussard, Boubker Bouzid, Marius Vasiliu and Roger Reynaud

A parallel algorithm for statistical multiword term extraction from very large corpora
Carlos Goncalves, Joaquim Silva and Jose Cunha

Vertex-centric Parallel Algorithms for Identifying Key Vertices in Large-scale Graphs
Bo Li, Zhuangliang Gao, Jianwei Niu, Yanfei Lv and Hong Zhang

HPCC PDC 4: Parallel and Distributed Computing
Tuesday 08:30, Room 1-D  Session Chair: Xin Li

A Parallelizing Matlab Compiler Framework and Run time for Heterogeneous Systems
Sam Skalicky, Sonia Lopez Alarcon, Marcin Lukowiak and Andrew Schmidt

Application Modeling for Scalable Simulation of Massively Parallel Systems
Eric Anger, Damian Dechev, Gilbert Hendry, Jeremiah Wilke and Sudhakar Yalamanchili
Distributed and Real-Time Query Framework for Processing Participatory Sensing Data Streams  
Chi Harold Liu, Zhen Zhang, Yue Huang and Kin K. Leung

GPregel: A GPU-Based Parallel Graph Processing Model  
Siyan Lai, Guangda Lai, Guojun Shen, Jing Jin and Xiaola Lin

**HPCC EES 1: Emerging Embedded Systems**  
*Monday 14:30, Room 2-A*  
*Session Chair: Weiwen Jiang*

Edwin Sha, Weiwen Jiang, Qingfeng Zhuge, Yang Lei, and Xianzhang Chen

**Buffer Filter: A Last-level Cache Management Policy for CPU-GPGPU Heterogeneous System**  
Songyuan Li, Jinglei Meng, Licheng Yu, Jianliang Ma, Tianzhou Chen and Minghui Wu

**Equidistant Memory Access Coalescing on GPGPU**  
Yulong Pei, Licheng Yu, Minghui Wu and Tianzhou Chen

**A Novel Fast Approach for Convolutional Networks with Small Filters Based on GPU**  
Wenbin Jiang, Yiming Chen, Hai Jin, Bin Luo and Ye Chi

**HPCC EES 2: Emerging Embedded Systems**  
*Tuesday 08:30, Room 2-A*  
*Session Chair: Lei Ju*

**AIMR: An Adaptive Page Management Policy for Hybrid Memory Architecture Involving NVM and DRAM**  
Zhiwen Sun, Zhiping Jia and Lei Ju

**Minimizing Update Bits of NVM-based Main Memory Using Bit Flipping and Cyclic Shifting**  
Xin Li, Meikang Qiu, Lei Ju and Zhiping Jia

**A Novel Memory Block Management Scheme for PCM Using WOM-code**  
Kun Ling, Zhiping Jia and Lei Ju

**Addressing Memory Wall Problem of Graph Computation in Reconfigurable System**  
Xu Wang, Linan Huang, Yongxin Zhu, Yipeng Zhou, Huwan Peng and Haifei Xiong

**HPCC EES 3: Emerging Embedded Systems**  
*Tuesday 08:30, Room 2-B*  
*Session Chair: Hongjun Dai*

**A Dynamic Contention-aware Application Allocation Algorithm for Many-core Processor**  
Chang Wang, Yongxin Zhu, Jiang Jiang, Xu Liu and Xing Han

**Fast Convolution Operations on Many-Core Architectures**  
Shigang Li, Yunquan Zhang and Chunyang Xiang

**Exploring Predictable Redundant Instruction Parallelism in Fault Tolerant Microprocessors**  
Hongjun Dai

**Communication-avoiding finite-differences seismic numerical kernels on multicore processors**  
Fabrice Dupros, Faiza Boulahya, Hideo Aochi and Philippe Thierry
HPCC SEC 1: Scientific and Engineering Computing  
Monday 14:30, Room 2-B  
Session Chair: Weiran Liu

Auditing and Revocation Enabled Role-Based Access Control over Outsourced Private EHRs  
Weiran Liu, Jianwei Liu, Xiao Liu, Qianhong Wu and Jun Zhang

SFDC: File Access Pattern Aware Cache Framework for High-performance Computer  
Wenrui Dong, Guangming Liu, Jie Yu and Wei Hu

Cross-Domain Sentiment Analysis of Product Reviews by Combining Learn-based and Lexicon-based Techniques  
Kaili Mao, Jianwei Niu, Xuejiao Wang, Lei Wang and Meikang Qiu

Request Squeezer: Mitigating Tail Latency through Pruned Request Replication  
Zuowei Zhang, Hailong Yang, Zhongzhi Luan and Depei Qian

HPCC SEC 2: Scientific and Engineering Computing  
Tuesday 08:30, Room 2-C  
Session Chair: Yibin Li

Semantic Process Mining Towards Discovery and Enhancement of Learning Model Analysis  
Kingsley Okoye, Abdel-Rahman Tawil, Usman Naeem and Elyes Lamine

Tracking Many Solution Paths of a Polynomial Homotopy on a Graphics Processing Unit in Double Double and Quad Double Arithmetic  
Jan Verschelde and Xiangcheng Yu

Binarization-based Human Detection with Hardware Reconfigurability  
Yibin Li, Zhiping Jia and Shuai Xie

Maximizing Hardware Prefetch Effectiveness with Machine Learning  
Saami Rahman, Martin Burtscher, Ziliang Zong and Apan Qasem

HPCC SEC 3: Scientific and Engineering Computing  
Tuesday 13:30, Room 1-B  
Session Chair: Yibin Li

A Stochastic Task Scheduling Algorithm Based on Importance-ratio of Makespan to Energy for Heterogeneous Parallel Systems  
Yuqing Yang, Xinqiao Lv, Hai Jin and Xiaofei Liao

Heterogeneous virtual machine consolidation using an improved grouping genetic algorithm  
Quanwang Wu and Fuyuki Ishikawa

Compiling HPC Kernels for the REDEFINE CGRA  
Kavitha Madhu, Saptarsi Das, Nalesh S., S K Nandy and Ranjani Narayan

Novel Routing Algorithm for minimum on Delay with Process Variation and Congestion in Asynchronous NoC  
Rabab Ezz-Eldin, Magdy A. El-Moursy and Hesham F. A. Hamed
HPCC SEC 4: Scientific and Engineering Computing
Tuesday 13:30, Room I-C wheelchair accessible
Session Chair: Songmao Zhang

Weiwei Shi, Yongxin Zhu, Jinkui Zhang, Xiang Tao, Gehao Sheng and Yufeng Chen

An analysis on occurrence probability of concurrency bugs based on combinatorial computing theory
Xu Jinchen, Guo Shaozhong, Wang Lei and Zhou Bei

Time-Dimension Communication Characterization of Representative Scientific Applications on Tianhe-2
Wenhao Zhou, Juan Chen, Zhuyuan Wang, Xinhai Xu and Yuhua Tang

Design and Architecture of Dell Acceleration Appliances for Database (DAAD): A Practical Approach with High Availability Guaranteed
Kai Yu, Yuxiang Gao, Peng Zhang and Meikang Qiu

HPCC SEC 5: Scientific and Engineering Computing
Tuesday 17:00, Room 2-A wheelchair accessible
Session Chair: Weiran Liu

Intelligent Usage Management of Shared Resources in Simultaneous Multi-Threading Processors
Yilin Zhang and Wei-Ming Lin

Load-distributed Linpack Implementation for Heterogeneous Clusters
David Rohr and Volker Lindenstruth

MPI+ULT: Overlapping Communication and Computation with User-Level Threads
Huiwei Lu, Sangmin Seo and Pavan Balaji

How small can it be?: The design of a cost-effective side-core for I/O Virtualization
Chung Lee and Peter Strazdins

HPCC SEC 6: Scientific and Engineering Computing
Tuesday 17:00, Room 2-D wheelchair accessible
Session Chair: Peng Zhang

Qi Ao, Shuai Chen, Longbing Zhang, Bin Liao and Jie Fu

Marriage Between Coordinated and Uncoordinated Checkpointing for the Exascale Era
Omer Subasi, Osman Unsal, Jesus Labarta and Ferad Zyulkyarov

TERN: A Self-Adjusting Thermal Model for Dynamic Resource Provisioning in Data Centers
Yuanqi Chen, Mohammed I. Alghamdi, Xiao Qin, Jifu Zhang, Minghua Jiang and Meikang Qiu

Querying large and expressive biomedical ontologies
Zhenzhen Gu and Songmao Zhang
HPCC MCCN 1: Mobile Computing and Communication Networks
Monday 14:30, Room 2-D

SwapBench: The Easy Way to Demystify Swapping in Mobile Systems
Xiao Zhu, Duo Liu, Liang Liang, Kan Zhong, Meikang Qiu and Edwin H.-M. Sha

DWDP A Double Warning Thresholds with Double Preemptive Scheduling Scheme for Wireless Rechargeable Sensor Networks
Chi Lin, Bingbing Xue, Zhiyuan Wang, Ding Han and Jing Deng

On Resource Scheduling of Wireless Converged Broadcasting and Cellular Networks with Popular Services Being Preferentially Delivered
Jian Xiong, Meikang Qiu, Lin Gui and Xia Li

Adaptive Assignment for Quality-Aware Mobile Sensing Network with Strategic Users
Ning An, Rui Wang, Zhongzhi Luan and Depei Qian

HPCC MCCN 2: Mobile Computing and Communication Networks
Tuesday 08:30, Room 2-D

Minimizing Energy Consumption with An CloneAnt-based Routing Algorithm for Communication Network
Yanqing Gao, Hua Wang, Runshui Zhu, Shanwen Yi, Chuangen Gao and Fuqiang Huang

A Space-efficient Parallel Algorithm for Counting Exact Triangles in Massive Networks
Shaikh Arifuzzaman, Maleq Khan and Madhav Marathe

Towards high-performance network processing in virtualized environments
Víctor Moreno, Rafael Leira, Iván González and Francisco Gomez Arribas

Static Node Center Hexagon Deployment in Hybrid Crowd Sensing Network
Shuang Ding, Xin He, Jicheng Wang, Wenyun Dai and Xilong Wang

HPCC OAA 1: Optimization Algorithms and Architectures
Monday 14:30, Room 2-C

Cost Minimization for Heterogeneous Systems with Gaussian Distribution Execution Time
Meikang Qiu, Yunjiang Jiang and Wenyun Dai

Optimization for Communication Energy Efficiency of Air-based Information Network while Satisfying Timing Constraints
Xiao Liu, Meikang Qiu, Xiaodong Wang, Weiran Liu and Jun Zhang

Parallel Dynamic Step Size Sphere-Gap Transferring Algorithm for Solving Conditional Nonlinear Optimal Perturbation
Shijin Yuan, Jinghao Yan, Bin Mu and Hongyu Li

Porting and optimizing SOAP2 on Loongson architecture
Qiuming Luo, Guoqiang Liu, Zhong Ming and Feng Xiao
HPCC OAA 2: Optimization Algorithms and Architectures
Tuesday 08:30, Room 1-B
Session Chair: Ying Li

Application Mapping and Scheduling for Network-on-Chip based Multiprocessor System-on-Chip with Fine-Grain Communication Optimization
Lei Yang, Weichen Liu, Weiwen Jiang, Mengquan Li, Juan Yi, Duo Liu and Edwin H. M. Sha

Optimizing Tasks Assignment on Heterogeneous Multi-core Real-time Systems with Minimum Energy
Ying Li, Jianwei Niu and Meikang Qiu

JolokiaC++: Optimizing Irregular Accesses for GPGPU
Vibha Patel, Sanjeev K. Aggarwal and Amey Karkare

Optimized Password Recovery for encrypted RAR in OpenCL
Xiaojing An, Yunquan Zhang and Haipeng Jia

HPCC WSSD 1: Web Service and Software Development
Tuesday 17:00, Room 1-A
Session Chair: Peng Zhang

Fast Numerical Evaluation for Symbolic Expressions in Java
Yueming Liu, Peng Zhang and Meikang Qiu

SiNUCA: A Validated Microarchitecture Simulator
Marco Antonio Alves, Carlos Villavieja, Matthias Diener, Francis Moreira and Philippe Navaux

Simulated Annealing to Generate Numerically Stable Real Number Error Correction Codes
Teresa Davies and Zizhong Chen

Low–Power Sensor Polling for Context–Aware Services on Smartphones
Jihe Wang, Meikang Qiu and Bing Guo

HPCC WSSD 2: Web Service and Software Development
Tuesday 17:00, Room 1-B
Session Chair: Xin Li

SLA-Aware Energy-Efficient Scheduling Scheme for Hadoop YARN
Ping Li, Lei Ju, Zhiping Jia and Xin Li

Inferring Information Propagation Over Online Social Networks: Edge Asymmetry and Flow Tendency
Jianwei Niu, Danning Wang, ChaoTong and Meikang Qiu

Discovering Event Evolution Chain in Microblog
Zhongyu Lu, Weiren Yu, Richong Zhang, Jianxin Li and Hua Wei

A New Matching Structure and Interval Partition on Content Based Publish/Subscribe System
Baojun Qiao, Ning Jiang, Zhipeng Wang and Fangfang Gao

HPCC Invited Paper CCNT 1: Cloud Computing and Networking Techniques
Tuesday 13:30, Room 2-A
Session Chair: Qin Liu

User-Controlled Security Mechanism in Data-Centric Clouds
Qin Liu, Guojun Wang and Jie Wu
Symbiot: Congestion-driven Multi-resource Fairness for Multi-User Sensor Networks  
Yad Tahir, Shusen Yang, Usman Adeel and Julie McCann

Time-Sensitive Virtual Machines Provisioning and Resource Allocation in Clouds  
Rehana Begam and Dakai Zhu

Cost-efficient Heterogeneous Data Transmission in Software Defined Vehicular Networks  
Zongjian He, Daqiang Zhang and Junbin Liang

**HPCC Invited Paper EST 1: Embedded System Techniques**

*Tuesday 13:30, Room 2-B*  
*Session Chair: Xiao Qin*

**Optimizing Emerging Storage Primitives with Virtualization for Flash Memory Storage Systems**  
Yi Wang, Lisha Dong and Zhong Ming

**HcDD: The Hybrid Combination of Disk Drives in Active Storage Systems**  
Shu Yin, Zhiyang Ding, Xiaojun Ruan, Xiaomin Zhu, Kenli Li and Xiao Qin

**Time-Triggered Mixed-Critical Scheduler on Single and Multi-processor Platforms**  
Dario Socci, Peter Poplavko, Saddek Bensalem and Marius Bozga

**An Efficient Technique for Chip Temperature Optimization of Multiprocessor Systems in Dark Silicon Era (Invited Paper)**  
Mengquan Li, Juan Yi, Weichen Liu, Wei Zhang, Lei Yang and Edwin H. M. Sha

**HPCC Invited Paper EST 2: Embedded System Techniques**

*Tuesday 13:30, Room 2-C*  
*Session Chair: Bo Li*

**A Data-oriented Method for Scheduling Dependent Tasks on High-density Multi-GPU Systems**  
Peng Zhang, Yuxiang Gao and Meikang Qiu

**Detecting Fault Injection Attacks on Embedded Real-time Applications: A System-level Perspective**  
Liang Wen, Wei Jiang, Ke Jiang, Xia Zhang, Xiong Pan and Keran Zhou

**Impact of Partitioning Cache Scheme on the Cache Hierarchy of SMT Processors**  
Samantha Kenyon, Sonia Lopez Alarcon and Julio Sahuquillo

**Gregarious Data Re-structuring in a Many Core Architecture**  
Sunli Shrestha, Joseph Manzano, Andress Marques, Stephane Zuckerman, Shuaiwen Leon Song and Guang Gao

**HPCC Invited Paper EAA 1: Engineering Architectures and Algorithms**

*Tuesday 13:30, Room 2-D*  
*Session Chair: Jinjun Xiong*

**A Framework for Learning-based DVFS Technique Selection and Frequency Scaling for Multi-core Real-Time Systems**  
Mahbub Ul Islam Fakhruddin and Man Lin

**A Hierarchical Resource Allocation Game for Heterogeneous Networks with Relays**  
Liang Liang, Gang Feng, Wen Wang, Yunjian Jia and Duo Liu

**Emergency Vehicle Signalling Using VANETs**  
Vandana Jayaraj and Hemanth C
A Resource Supply-demand based Approach for Automatic MapReduce Job Optimization  
Jinjun Xiong, Dzung Phan and David Kung

**HPCC Invited Paper EAA 2: Engineering Architectures and Algorithms**

*Tuesday 17:00, Room 2-C*  
*Session Chair: Zili Shao*

**SmartBackup: An Efficient and Reliable Backup Strategy for Solid State Drives with Backup Capacitors**  
Min Huang, Yi Wang, Liyan Qiao, Duo Liu and Zili Shao

**Electronic Health Record Error Prevention Approach Using Ontology in Big Data**  
Keke Gai, Meikang Qiu, Li-Chiou Chen and Meiqin Liu

**The Potential of the Intel Xeon Phi for Supervised Deep Learning**  
Andre Viebke and Sabri Plana

**Bandwidth-aware Energy Efficient Routing with SDN in Data Center Networks**  
Guan Xu, Bin Dai, Benxiong Huang and Jun Yang

**HPCC Short Paper CCN 1: Cloud Computing and Networks**

*Tuesday 15:10, Room 2-A*  
*Session Chair: Yunjiang Jiang*

**Cluster Scheduler on Heterogeneous Cloud**  
Xiao Ling, Jiahai Yang, Dan Wang and Ye Wang

**Communication Energy Constrained Spare Core on NoC**  
Naresh Reddy

**Dependability Implementation in Cloud Computing with the Cloud Broker Architecture**  
Wiem Abderrahim and Zied Choukair

**Research on Campus Mobile Model Based on Periodic Purpose For opportunistic network**  
Xin He, Chunxi Wang, Dehong Chen, Keke Gai, Tianxu Liu and Lin Bai

**Agent and Spatial Based Parallelization of Biological Network Motif Search**  
Matthew Kipps, Wooyoung Kim and Munehiro Fukuda

**Run Time Approximation of Non-blocking Service Rates for Streaming Systems**  
Jonathan Beard and Roger Chamberlain

**HPCC Short Paper CCN 2: Cloud Computing and Networks**

*Tuesday 15:10, Room 2-B*  
*Session Chair: Ruixuan Li*

**An Improved Hybrid Time Synchronization Approach in Wireless Sensor Networks for Smart Grid Application**  
Fen Li and Guanghui He

**NV-CFS: NVRAM-Assisted Scheduling Optimization for Virtualized Mobile Systems**  
Dan Zhang, Duo Liu, Liang Liang, Lei Yao, Kan Zhong and Zili Shao

**A high level framework to develop and run e-science applications on Cloud infrastructures**  
Nabil Abdennadher and Mohamed Ben Belgacem

**Towards Optimal Task Distribution on Computer Clusters with Intel MIC Coprocessors**  
Chenggang Lai, Miaoqing Huang and Genlang Chen
Mining Relations between Courses and Research Directions from Educational Data
Xiaopeng Gao, Shuai Ruan, Xuejiao Wang and Shufan Ji

**HPCC Short Paper ESEC 1: Embedded Systems and Engineering Computing**

*Tuesday 15:10, Room 1-A  Session Chair: Duo Liu*

**Having Memory Storage Under Control of a File System**
Shuichi Oikawa

**Using Artificial Neural Network for Predicting Thread Partitioning in Speculative Multithreading**
Yuxiang Li, Yinliang Zhao and Huan Gao

**GPU-Memory Coordinate Energy Saving Approach Based on Extreme Learning Machine**
Junke Li, Bing Guo, Yan Shen, Deguang Li, Jihe Wang and Yanhui Huang

**TLC-FTL: Workload-aware Flash Translation Layer for TLC/SLC Dual-Mode Flash Memory in Embedded Systems**
Lei Yao, Duo Liu, Kan Zhong, Linbo Long and Zili Shao

**Shared Write Buffer to Support Speculative Multi-Threading**
John Ye and Tianzhou Chen

**HPCC Short Paper ESEC 2: Embedded Systems and Engineering Computing**

*Tuesday 15:10, Room 1-B  Session Chair: Jun-Jie Peng*

**Real-Time Memory Controller for Embedded Multi-core System**

**Deploying OpenMP Task Parallelism on Multicore Embedded Systems with MCA Task APIs**
Peng Sun, Sunita Chandrasekaran, Suyang Zhu and Barbara Chapman

**FPGA Design and Implementation for Real-Time Electromagnetic Transient Simulation System**
Xing Zhang, Guanghui He and Xiaoxin Zhou

**Game based Strategic Security Resource Allocation Algorithm in Secured Smart Environments**
Youngjae Park and Sungwook kim

**Preventing Access to Residual Data Exposed by Packet Expansion Operations**
Ralph Duncan, Kenneth Ross, Jim Frandeen and Alfredo Chorro-Rivas

**HPCC Short Paper ESEC 3: Embedded Systems and Engineering Computing**

*Tuesday 15:10, Room 1-C  Session Chair: Laurence Tianruo Yang*

**Flexible Linear Algebra Development and Scheduling with Cholesky Factorization**
Azzam Haidar, Asim Yarkhan, Chongxiao Cao, Piotr Luszczek, Stanimire Tomov and Jack Dongarra

**Worst-Case Execution Time Analysis of Intel Atom D510**
Matthew Loach, Pradeep Subedi and Wei Zhang

Vector Folding: improving stencil performance via multi-dimensional SIMD-vector representation
Charles Yount

A Case Study on Task-Level Parallel Implementation of H.264 Decoder on Multiprocessor Platforms
Weichen Liu, Xiaohao Lin, Chunming Xiao, Jie Dai, Xianlu Luo and Dan Zhang

A General Space-filling Curve Algorithm for Partitioning 2D Meshes
Aparna Sasidharan, John Dennis and Marc Snir

### HPCC Short Paper PDA 1: Parallel and Distributed Architecture and Algorithm

**Tuesday 15:10, Room 2-D**

**Session Chair:** Qin Liu

User Satisfaction Based Dynamic Priority Assignment Algorithm for Internet of Things
Gai Wang and Yongyan Wang

LiveIndex: A distributed online index system for temporal microblog data
Huang Haifei, Li Jianxin, Zhang Richong, Yu Weiren and Ju Wuyang

A Grid-based k-Nearest Neighbor Join for Large Scale Datasets on MapReduce
Miyoung Jang, Youngsung Shin and Jae Woo Chang

A Parallel Framework for Object Detection and Recognition for Secure Vehicle Parking
Zahid Mahmood, Muhammad Usman Khan, Muhammad Jawad, Samee Ullah Khan and Laurence T. Yang

Marbor: A Distributed Graph Data Storage and Processing Framework
Wei Zhou

### HPCC Short Paper PAM 1: Performance Analysis and Measures

**Tuesday 15:10, Room 2-C**

**Session Chair:** Laizhong Cui

Hardware Thread-Level Speculation Performance Analysis
Ying-Chieh Wang, Ihsin Chung and Cherung Lee

Performance Evaluation of Heterogeneous Servers Allocation Disciplines in Networks with Retrial
Nawel Gharbi, Leila Charabi and Lynda Mokdad

Performance Improvement of Seismic Analysis in a Large Scale Interactive Visualization
Hui Wang and Ping Lv

Design and Performance Analysis of Antenna Array in LTE-Advanced
Hun Choe, Sang Mi Moon, Myeonghun Chu and Intae Hwang

Performance Profiling of VMs on NUMA Multicore Platform by Inspecting the Uncore Data Flow
Qiuming Luo, Feng Xiao, Yuanyuan Zhou and Zhong Ming
**HPCC Poster:**

*Session Chair: Hui Zhao*

Cognitive Radio Resource Management Scheme based on VCG mechanism and Rubinstein Bargaining Model  
Youngjae Park and Sungwook Kim

**Improving CPU Service Offerings in Apache CloudStack**  
Fernando Gomez-Folgar, Antonio Garcia-Loureiro and Tomás F. Pena

A Flexible Cluster System for the Management of Virtual Clusters in the Cloud  
Fernando Gomez-Folgar, Guillermo 100 Indalecio, Antonio Garcia-Loureiro and Tomás F. Pe

Optimization of LevelDB by Separating Key and Value  
Jian Zhang, Lei Wang and Yulong Zhao

A Crowd Sourcing Service Model for Optimizing User-Desired Storage Resource Scheduling  
Huigui Rong, Jianfang Li, Bingguo Chang, Zheng Qin and Fei Long

Temperature, Voltage, and Aging Effects in Ring Oscillator Physical Unclonable Function  
Muslim Mustapa and Mohammed Niamat

Towards Energy-Aware Placement of Real-Time Virtual Machines in a Cloud Data Center  
Nima Khalidzad, Hamid Reza Faragardi and Thomas Nolte

Optimized Inter-domain Communications Among Multiple Virtual Machines Based On Shared Memory  
Jian Wan, Hongyuan Wu, Congfeng Jiang, Xianghua Xu, Yunfa Li, Wei Zhang, Jilin Zhang and Zujie Ren

Millipedes: Distributed & Set-Based Sub-Task Scheduler of Computing Engines Running on Yarn Cluster  
Kebing Wang, Zhaojuan Bian and Qian Chen

A Group Order-Preserving Encryption Scheme based on Periodic Functions for Efficient Query Processing on Encrypted Data  
Lee Hyunjo, Choi Munchol and Chang Jae-Woo

Survey of Big Data-as-a-Service Type  
Yunkon Kim, Yong-Hyun Kim, Ga-Won Lee and Eui-Nam Huh

Elena Troubitsyna and Linas Laibinis. Towards Visualisation of Resilience Assessment for Large-Scale Systems  
Elena Troubitsyna and Linas Laibinis
Jim Jeffers is a Principal Engineer and Engineering Manager in Intel's Enterprise and HPC Platform Group. Jim joined Intel in 2008 focused on the many-core Intel® Xeon Phi™ product family development. Jim's experience includes software design and technical leadership in high performance computing, visual computing, digital television, and data communications. He currently leads development for Intel's parallel software defined visualization solutions. Jim has coauthored and coedited several books on parallel software development including Intel® Xeon Phi™ Coprocessor High Performance Programming (Morgan Kaufmann, 2013) and High Performance Parallelism Pearls (Morgan Kaufman, Volume 1, 2014; Volume 2, 2015).

Get the latest information on industry progress for an open-source, high performance, high fidelity software-defined visualization rendering stack on Intel® Xeon® processors and the Intel® Xeon Phi™ product family without the need for specialized hardware such as GPUs. Hear how the ever-growing data sizes used in the modeling and simulation of complex scientific phenomena drives a need to visualize this data faster and with higher quality to maximize scientific understanding. Other topics in this session include: (1) Industry-driven software solutions that support the need to minimize power usage and increase the efficiency of cluster resources while enabling better performance, flexibility and higher-fidelity visual solutions. (2) Benefits to visualization using the Next Generation Intel Xeon Phi processor (codenamed Knights Landing).
Privacy Challenges in Big Data Systems

Dr. Fei is a Staff Software Engineer and tech lead at Google Inc. His expertise is Big Data infrastructure and privacy. He currently leads an R&D team working on the frontiers of privacy in Big Data systems. Prior to that, he was the tech lead of Google’s Sawzall solution. Prior to Google, he was a senior R&D engineer at Synopsys Inc. His team developed industry’s leading technology for defect detection and analysis in large-scale designs. Dr. Fei received Ph.D. in Electrical and Computer Engineering from Purdue University, West Lafayette.

With the recent rise of social networks, smart devices, sensor networks, wearable computing, and internet of things, enormous amount of private user information is collected, stored, processed, and potentially shared. Various government agencies and privacy advocate groups have been more vigilant than ever in working with tech industry to establish the regulations to protect user privacy, and to educate users of potential privacy risks. Protecting user privacy in Big Data systems is critical as such systems are typically the confluence of data flows producing and consuming private user information.

In this talk, we will go over the rapidly evolving frontiers of privacy in the internet / mobile computing industry, privacy constraints of Big Data implementations, and share our firsthand experience in protecting user privacy in Google’s Big Data systems. We will also discuss some open challenges in privacy.
Dr. Stan Posey
HPC Industry
Market
Development, NVIDIA

Application Readiness for the Pre-Exascale Phase

Stan Posey joined NVIDIA in 2009 with more than 20 years of experience in the HPC industry. Mr. Posey began his career as an engineering analyst in applied HPC at the U.S. DOE Oak Ridge National Laboratory, and later CAE consultant CD-adapco. However, limitations posed by meshing software of those days along with excessive compute times, motivated a transition to the vendor community to aid in improvements of HPC solutions. Mr. Posey held technical roles in applications engineering and industry development during 17 years at SGI, and contributed to advances in parallel I/O for HPC application software during 3 years at Panasas. At NVIDIA, Mr. Posey is an HPC Program Manager where he leads the company’s strategy on HPC solutions for the domains of CFD and Earth system modeling.

Computational efficiency with increased focus on performance-per-energy-cost has become the overarching driver behind architectural considerations for Exascale HPC. The development of scientific and engineering application software that achieves full potential from such Exascale systems will require a level of hardware/software co-design that is a relatively new approach in conventional HPC. GPUs are a centerpiece of the first pre-Exascale systems announced in the USA under the U.S. Department of Energy CORAL partnership, and are a key component of co-design collaborations that will strive for accelerated application readiness by system deployment in 2017.

This presentation will first examine the motivation and progress of GPU-based heterogeneous system architectures for the pre-Exascale phase of HPC. The second topic will introduce the requirements for extraction of fine-grain parallelism of application software and current state of GPU-accelerated modelling and simulation applications with review of the programming strategies deployed. The third and final topic will provide roadmaps of GPU hardware and system software, and interoperability with these new host CPU platforms.
Combining Process Algebra with Logic Programming – A Calculus for knowledge based Orchestration

Ruqian Lu is a professor of computer science of the Institute of Mathematics, Academy of Mathematics and Systems Science, at the same time an adjunct professor of Institute of Computing Technology, Chinese Academy of Sciences and Peking University. He is also a fellow of Chinese Academy of Sciences. His research interests include artificial intelligence, knowledge engineering, knowledge based software engineering, formal semantics of programming languages and quantum information processing. He has published more than 180 papers and 10 books. He has won two first class awards from the Chinese Academy of Sciences and a National second class prize from the Ministry of Science and Technology. He has also won the 2003 Hua Loo-keng Mathematics Prize from the Chinese Mathematics Society and the 2014 lifetime achievements award from the China’s Computer Federation.

This talk presents Knorc – a calculus for KNowledge based ORchestration, which is a conservative extension of the Orc calculus. Orc is, as claimed by its authors, a language for wide area computation and has been developed at University of Dallas. It is simple and powerful with site calls as program units and four combinators to compose them. There was quite a lot of following up works along this line. Knorc is yet another extension of Orc in direction of knowledge processing. The main new ingredient is logic programming whose combination with process algebra is a major technical challenge to the design of Knorc. Besides introducing new possibilities of implementing site calls, the advantages of this combination include better structuredness of programs, separation of knowledge content from control flow and reusability of knowledge. The second main ingredient is the availability of a set of different parallel programming paradigms, which makes Knorc a process algebra not only with logic programming facilities, but also with powerful parallel logic programming facilities. In particular, it is possible to do massive parallel programming in Knorc. The third main ingredient is the introduction of a specific data type – the abstract knowledge sources to increase its knowledge processing power. While Orc has no data types at all, several extension works in the literature have introduced different data types, e.g. the XML data type. The introduction of abstract knowledge sources makes Knorc a language based on Open World Assumption, rather than Closed World Assumption. We have formalized the syntax and semantics of Knorc. A first implementation of Knorc is underway.
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<th>Dr. Yung-Chin Fang</th>
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<td>Senior Principle Engineer, Dell Inc</td>
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<td><strong>Dr. Kevin D. Johnson</strong></td>
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<td>Professional Services Technical Consultant, IBM</td>
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Pushing the Frontier of Software Engineering: 
Big-Applications as Eco-Systems of Global Scale

In this talk, we discuss the challenges in engineering large scale high performance applications. We will present a number of significant use-cases in different industries (financial, health, pharma, distribution, retail, and the like) that defy our ability to engineer systems the right way. We will characterize the underlying problems and argue for the need for new paradigm in the way we approach application design and development. We will discuss how engineers in other fields dealt with such complexity and the lessons learned from their techniques. We will propose practical approaches that I have been using to analyze and design for problems of eco-system scale.
The Requirement and Impact of Petascale Computing in Automotive Simulation

Greg has worked in the high performance computing (HPC) field for over 25 years, most recently with Cray, Inc as the Manufacturing Segment Manager. Greg's primary focus has been on application performance on HPC architectures. This has involved close cooperation with application developers and users to improve the real performance for production environments. Prior to Cray, Greg worked for IBM for 10 years in the HPC team and 16 years at Cray Research in the Application department. Greg has a MS in Structural Engineering from the University of Minnesota and has completed the "Executive Management Training" program in the Haas School of Business, Univ. of California, Berkeley.

The Automotive industry has seen a dramatic growth in HPC compute capability and "Petascale" compute environments are increasing common. This presentation will cover the simulation requirements which are driving this growth and how the CAE application developers are responding. It will include examples of CAE application performance from Petascale system and how this compute power impacts the CAE environment. Also this level of compute power generates huge volumes of data and increases the need for data analytics on not only the simulation results but also test data, manufacturing data, and other sources of information.
General Information

Registration Desk

The Registration Desk will be open to assist you at the following times:

- Monday, 24 August 2015, 08:00 – 18:00
- Tuesday, 25 August 2015, 08:00 – 18:00
- Wednesday, 26 August 2015, 08:00 – 17:00

Location: Main Lobby.

Conference materials, name badges, and other proceedings will be distributed at the Registration Desk.

Name Badges

All delegates, sponsors, speakers, and attendees of HPCC/ICESS/CSS 2015, associated workshops, and summit will be provided with a name badge, to be collected upon registration. This badge must be worn at all times as it is your official pass to all sessions of the conferences, lunches, morning and afternoon teas, and banquets.

Social Events

Welcome Reception
Banquet Dinner

Presentation Instruction

You are required to arrive at the room (in which you will deliver your talk) at least 15 minutes before the commencement of the session. Upon arrival please confirm your attendance with the Session Chair and familiarize yourself with the venue. Please bring with you a single paragraph summary, including your name (as you would like to be introduced), affiliation and research interests (maximum 100 words). Please present this to the session Session Chair upon arrival, for use for introductory purposes, prior to your talk. Upon arrival, please copy your slides file to the presentation computer. If you plan to use your own equipment, please ensure it is ready to go prior to the session commencing, since there is very little time between presentations. If you have requested optional equipment, ensure that is in the room. For all assistance, please speak to the Session Chair.

Message Board

Any program changes or urgent announcements from the secretariat and private messages will be posted on the message board in the registration area. Please check the message board occasionally.
Venue

HILTON NEWARK AIRPORT
1170 SPRING STREET, ELIZABETH, NEW JERSEY, 07201-2114, USA
TEL: +1-908-351-3900 FAX: +1-908-351-9556
Floor Maps

Room 1-C
Room 1-B
Room 1-A
Room 1-D
Ball Room
Room 2-C
Room 2-B
Room 2-D
Room 2-A