

The Technology behind PlayStation®2



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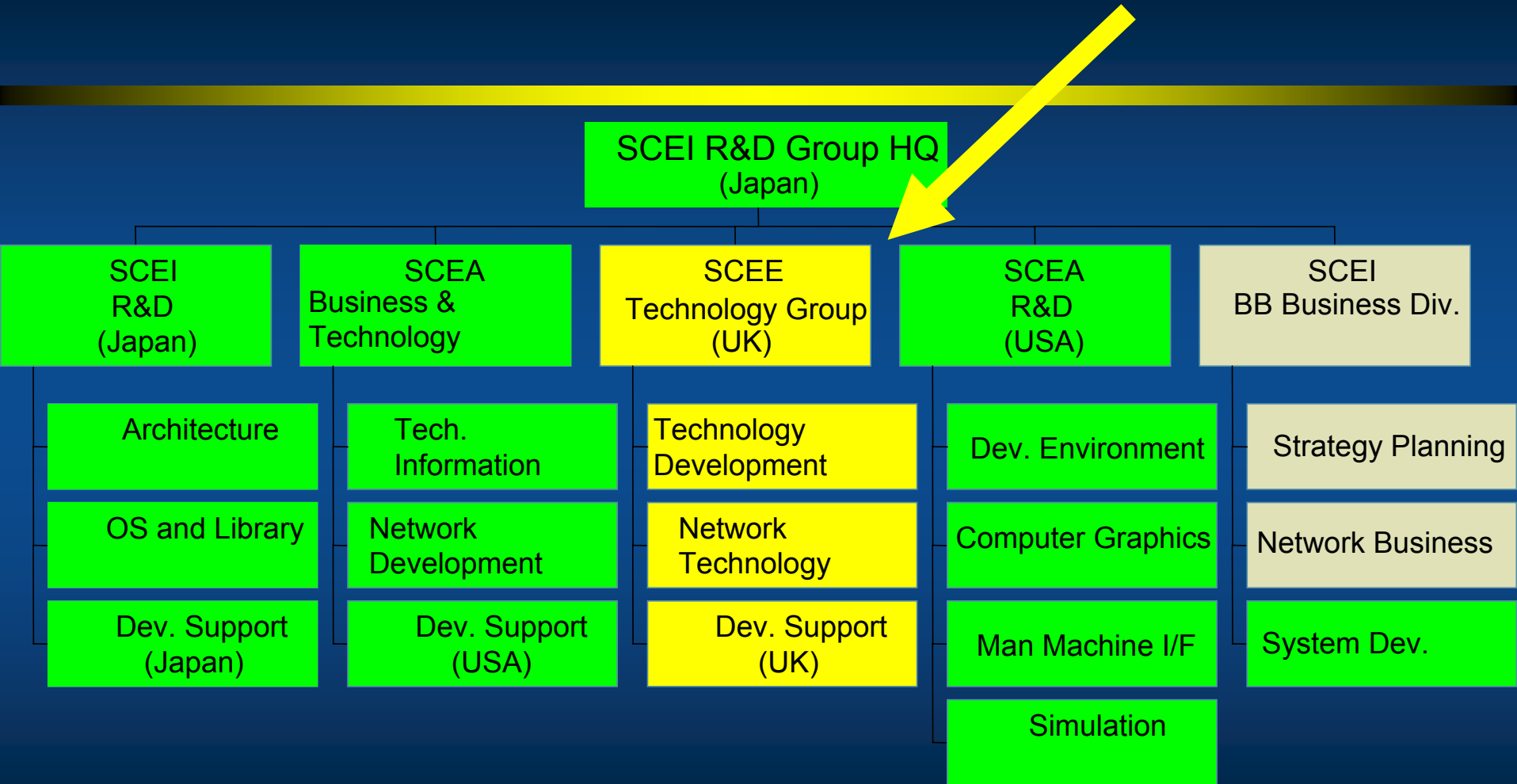


In this presentation

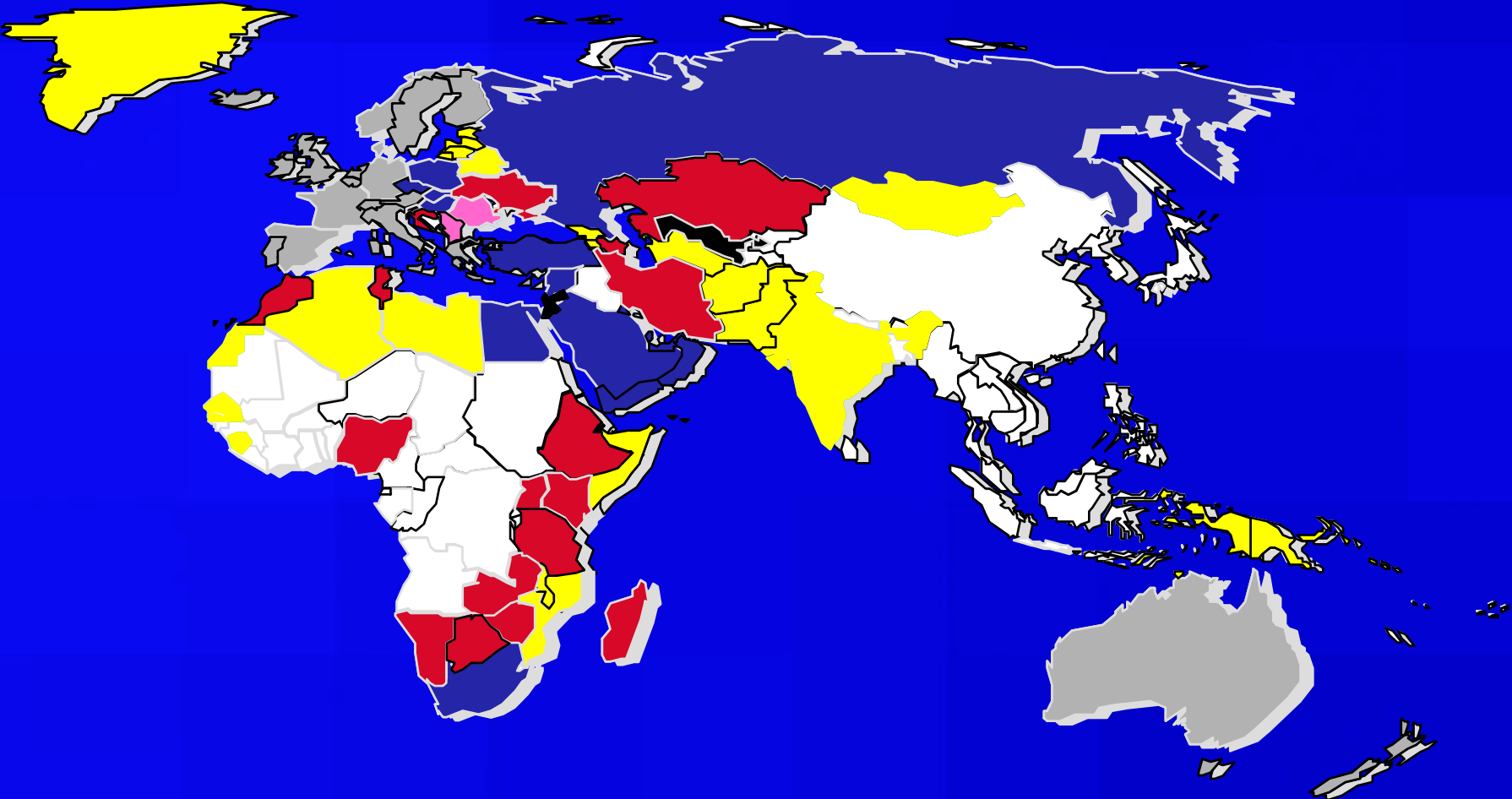
- Sony Computer Entertainment Overview
- Technical aspects of PlayStation 2
- The Future for PlayStation



Who Am I ?



Sony Computer Entertainment "Europe"



- Launch - Apr 96
- May 96 - Apr 97
- May 97 - Apr 98
- May 98-Apr 99
- May 99- Jan 02



PlayStation 2

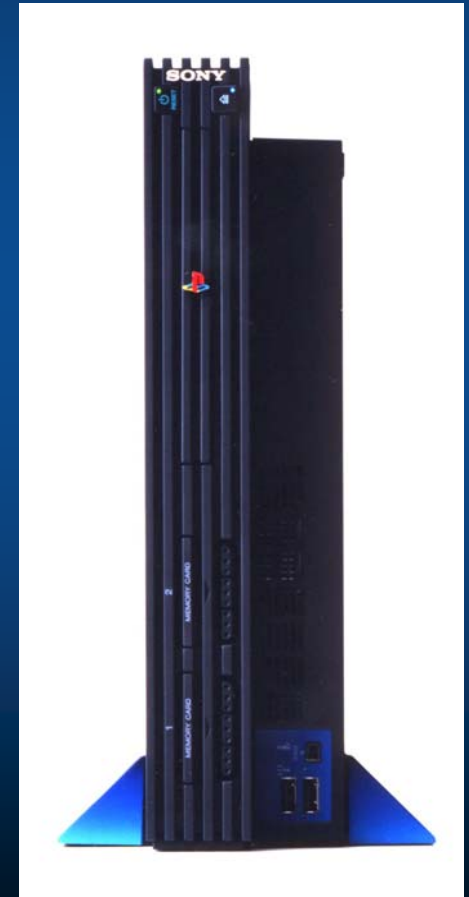


COMPACT
disc

DVD
VIDEO

DD DOLBY
DIGITAL

dts
DIGITAL OUT



European Launched 24 November 2000

Where are we now ?

September 2002 – 40 million PS2s shipped worldwide (12+ million to SCEE region)

BUT ... sales are seasonal – vast majority in Christmas season

Sales are running at 2.4x original PlayStation at the same point of lifecycle



Manufacturing Technology



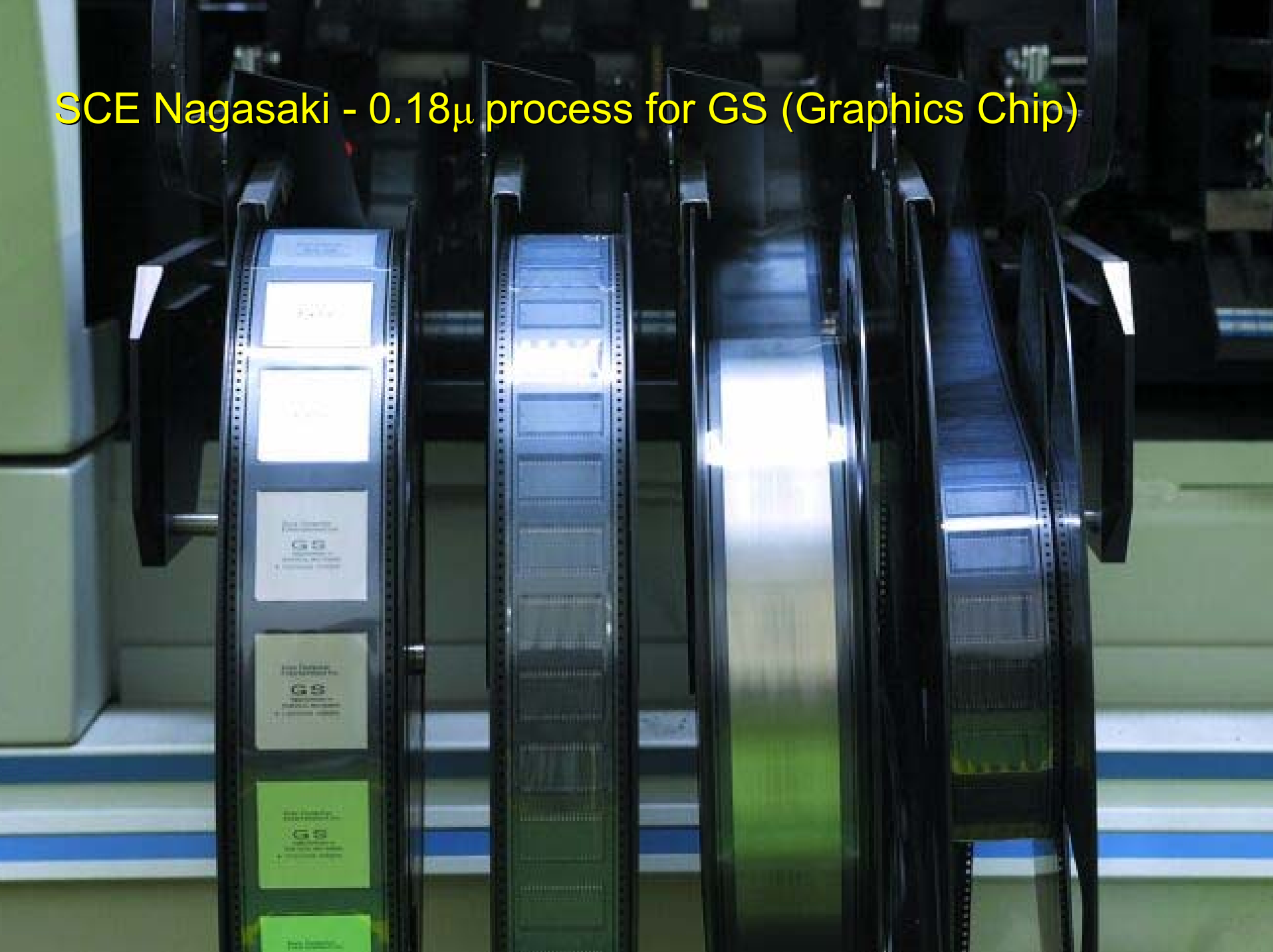
A peek inside the factory



EE (Main Processor) – Joint Fab with Toshiba in Ohita (0.18 μ)



SCE Nagasaki - 0.18 μ process for GS (Graphics Chip)





And what about the software ?



Disc manufacturing (CD and DVD)

- All Disc manufacturing carried out by Sony DADC in Salzburg, Austria
- Includes proprietary copy control solutions
- PS2 discs are serialized
- “Just-in-time” ordering



The Technology inside the machine ...



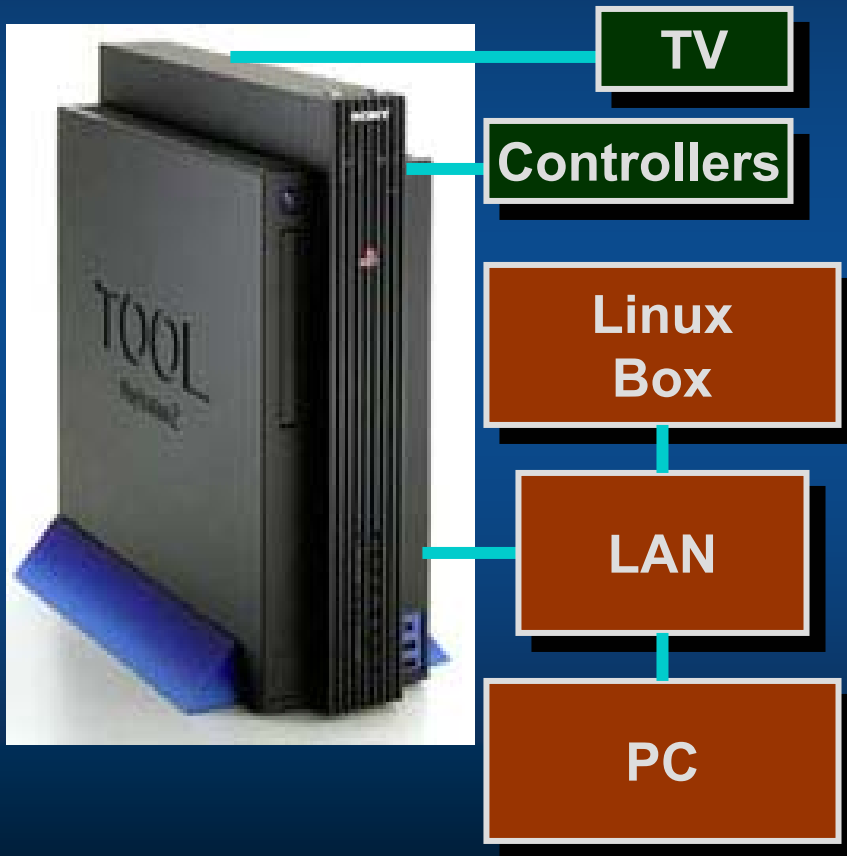
Technical Aspects of PlayStation 2

- The PlayStation 2 Development Environment
- System Architecture
 - The Emotion Engine (EE)
 - The Graphics Synthesiser (GS)
 - The IO Processor (IOP)



Professional Development Environment

The TOOL



- Use the Linux-based tools that come with the TOOL
- With a Linux box you can either:
 - develop and compile on the Linux Box
 - use the Linux Box purely for compilation and develop in your favourite Windows Editor



Developing at home – PS2 Linux

- PlayStation 2 branded USB keyboard & mouse
- 10/100 Ethernet Adapter
- 40GB Hard Disk
- Monitor cable
- 2 x install DVD's
 - Linux
 - Hardware Manuals
 - Tools, Examples
- Simple EULA
- Launched: 22 May '02
- € 249 (excl. VAT and Shipping) from <http://www.linuxplay.com/>



Here comes the science bit ...

System Architecture



PlayStation2

- 128-bit CPU core “Emotion Engine”
- GS “Graphics Synthesizer”
- SPU2 “Dynamic Sound Processor”
- I/O Processor (USB, i.Link)
- DVD/CD ROM disc system

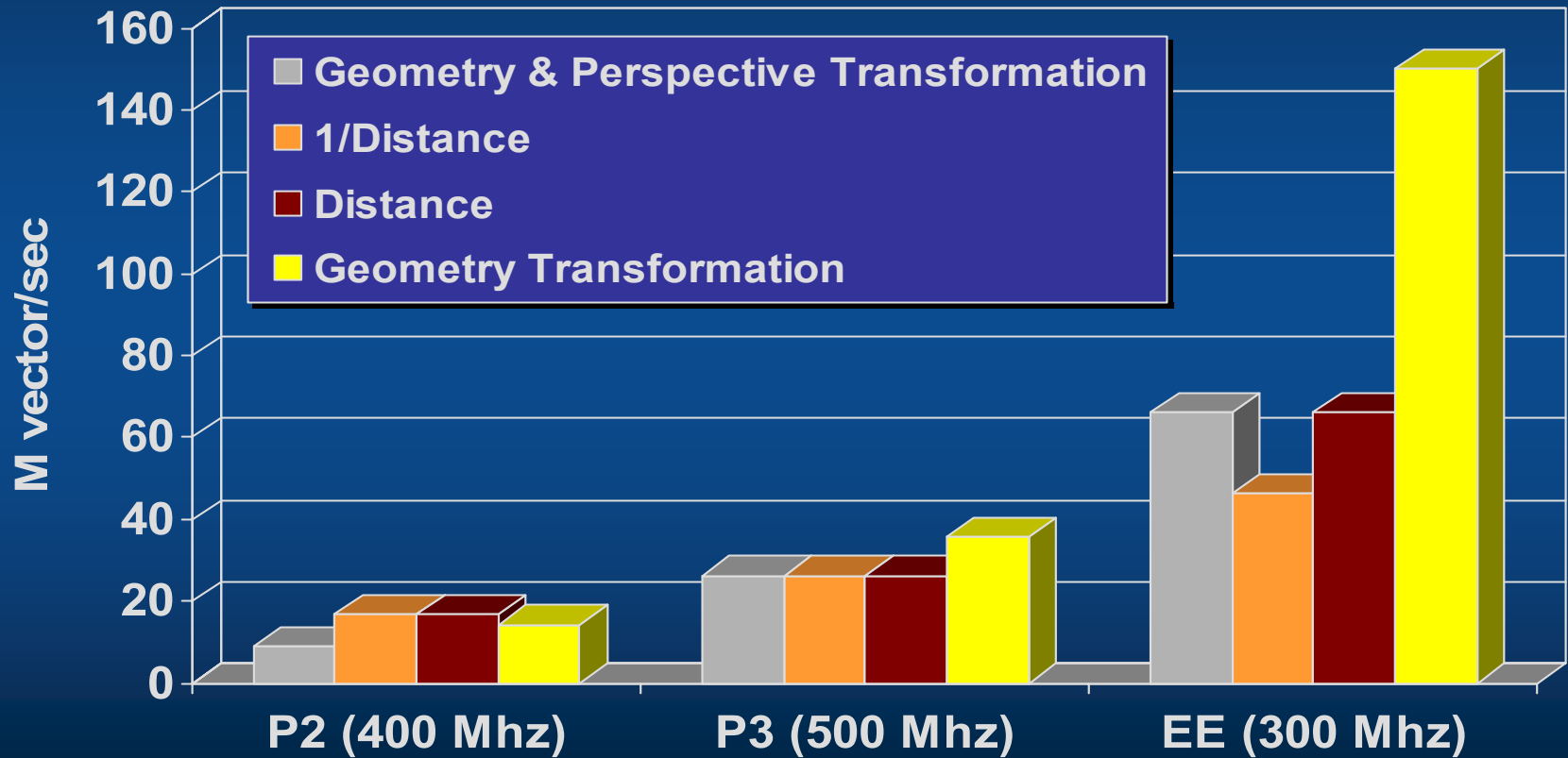


The Emotion Engine - Specs

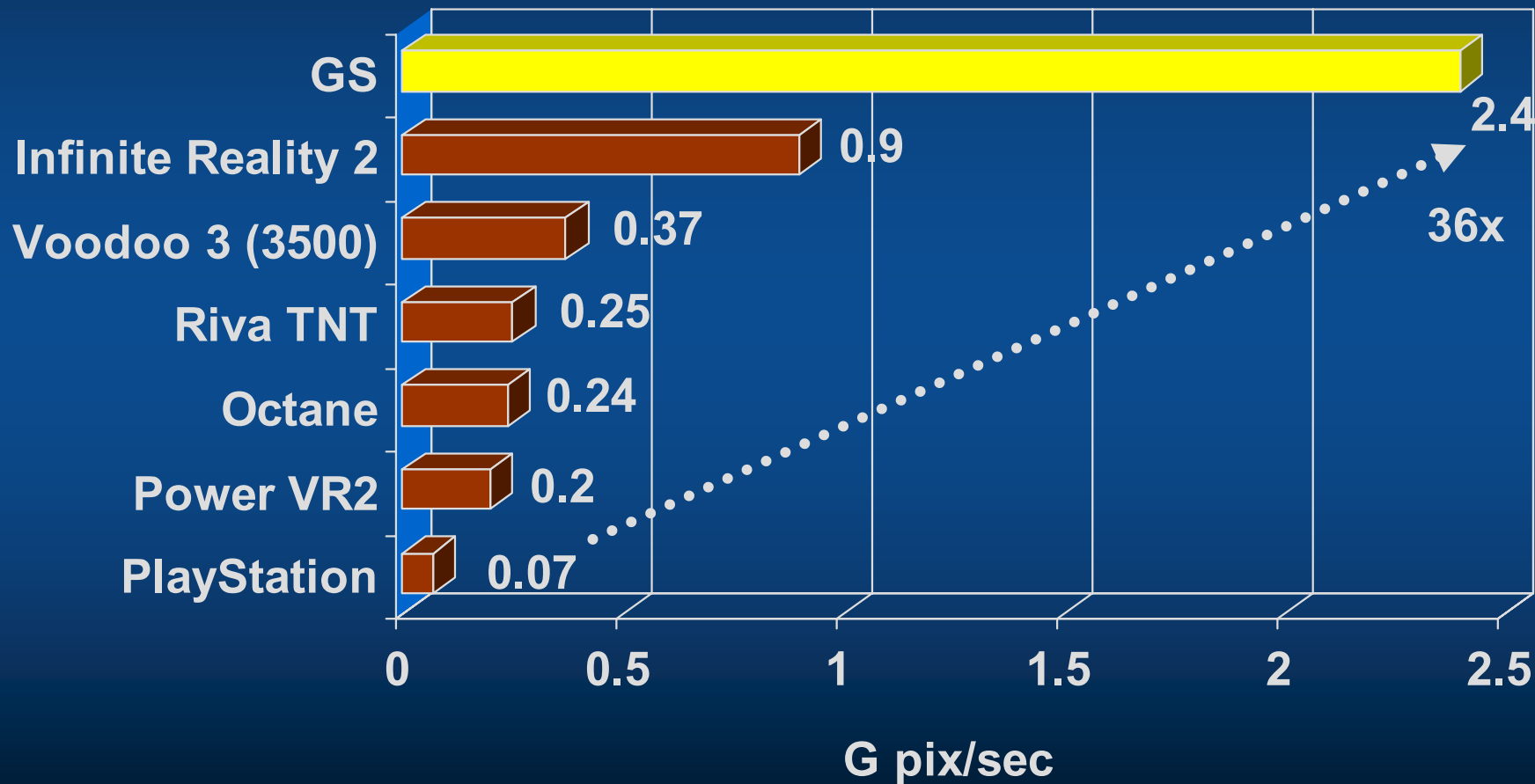
- CPU Core 128 bit CPU
- System Clock 300MHz
- Bus Bandwidth 3.2GB/sec
- Main Memory 32MB (Direct Rambus)
- Floating Point Calculation 6.2 GFLOPS
- 3D Geometry Performance 66 Million polygons/sec
- Image Processor Unit MPEG2



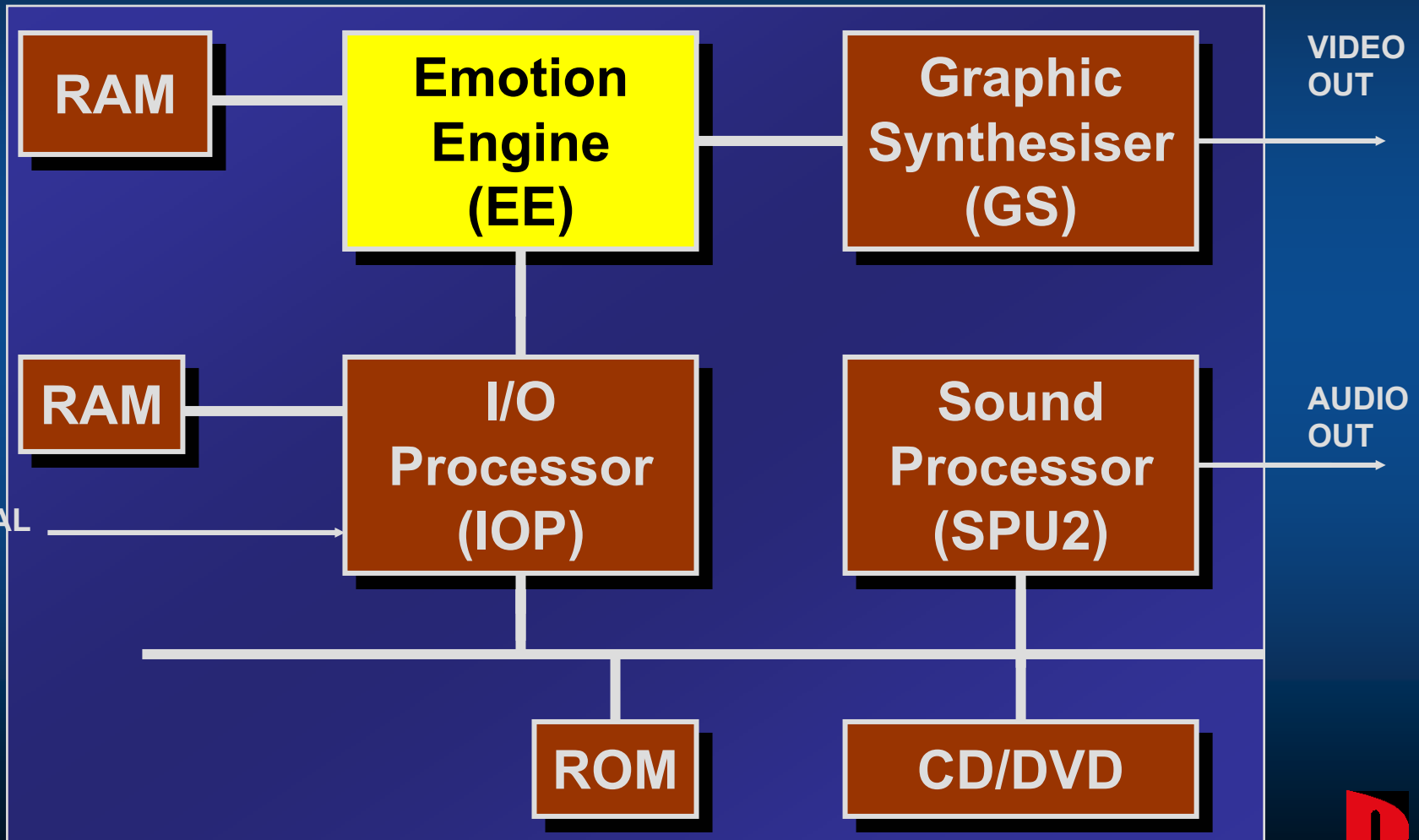
Floating Point Vector Performance ...



Pixel Fill Rate

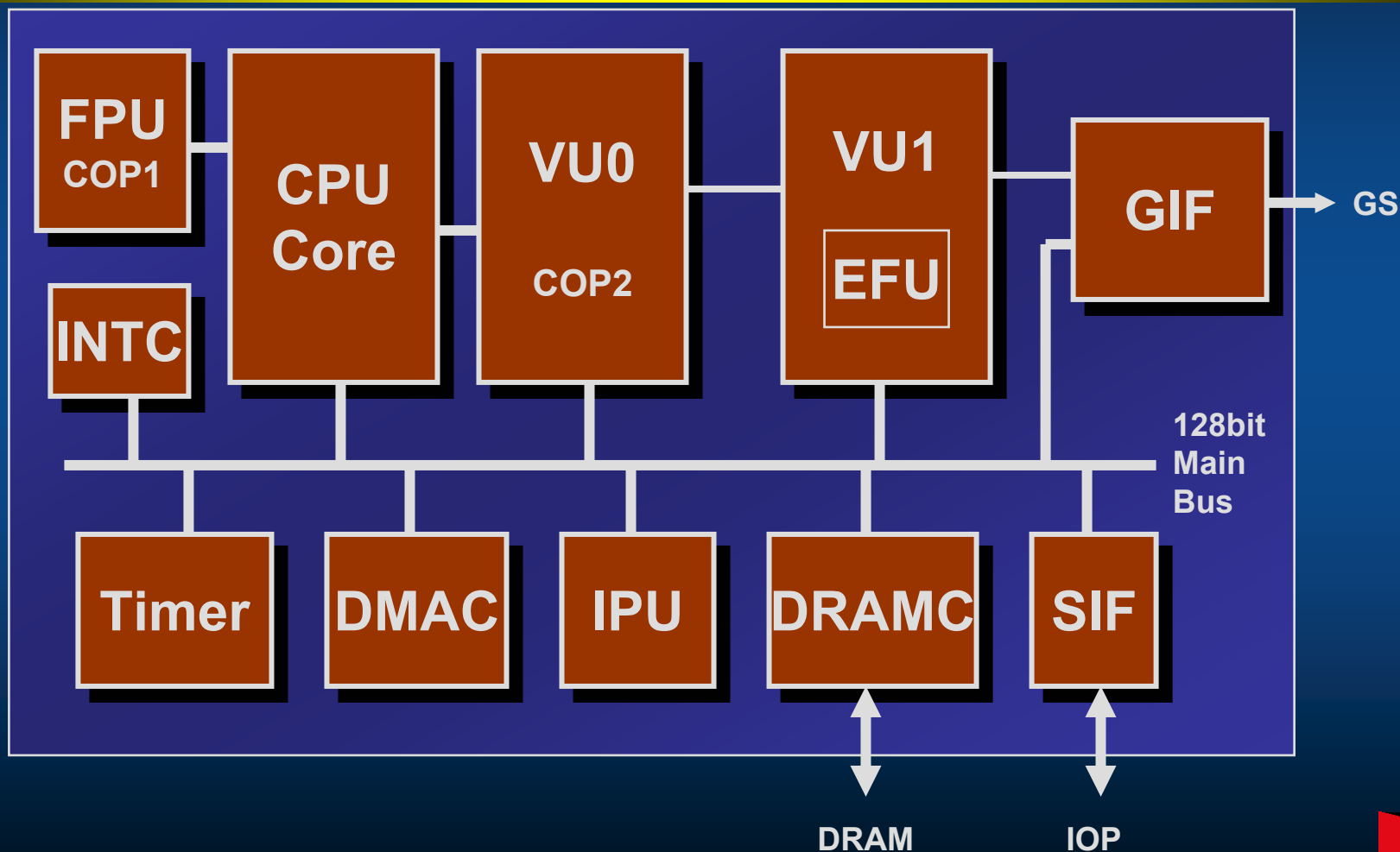


System Architecture



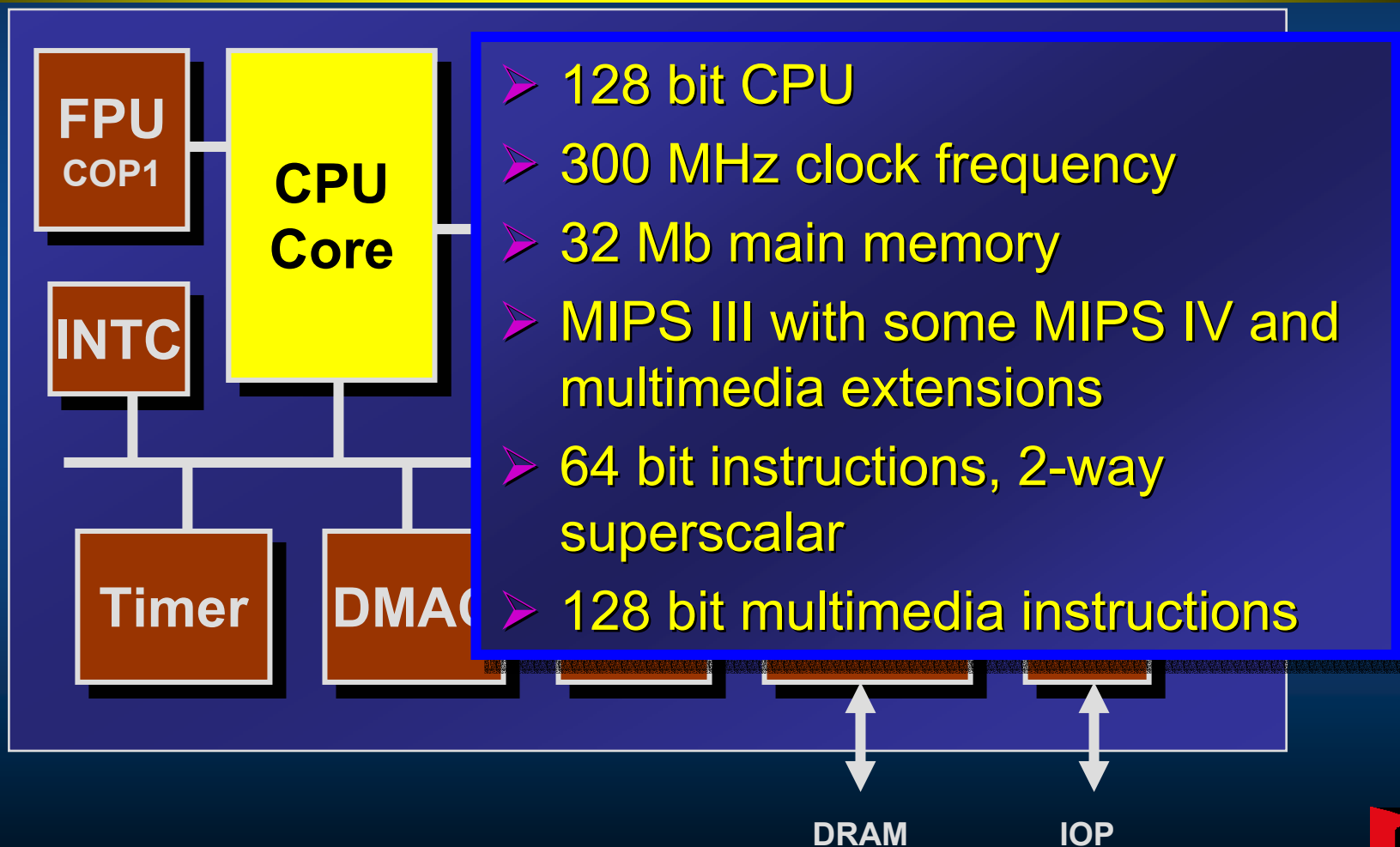
Emotion Engine architecture

Overview



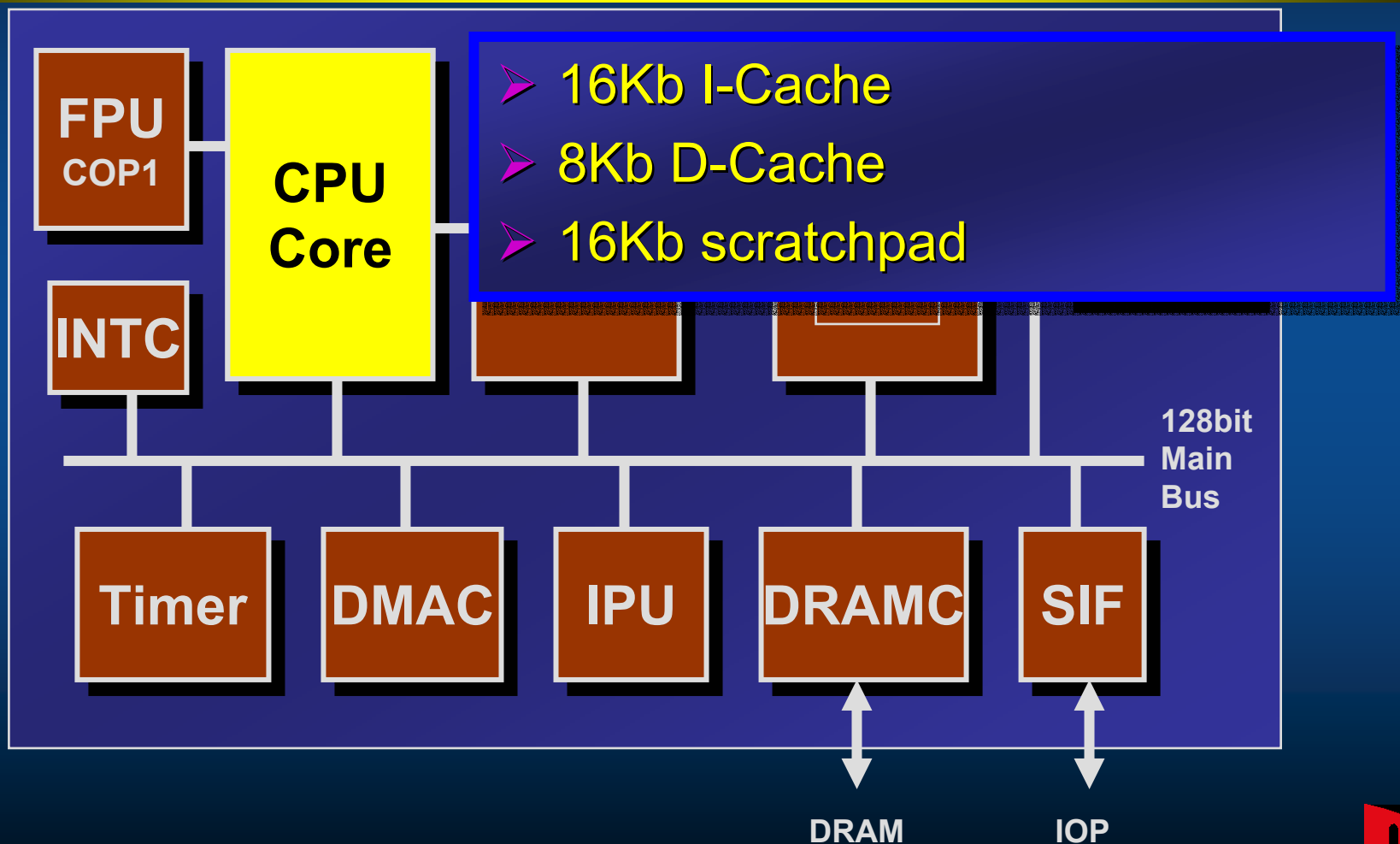
Emotion Engine architecture

CPU Core



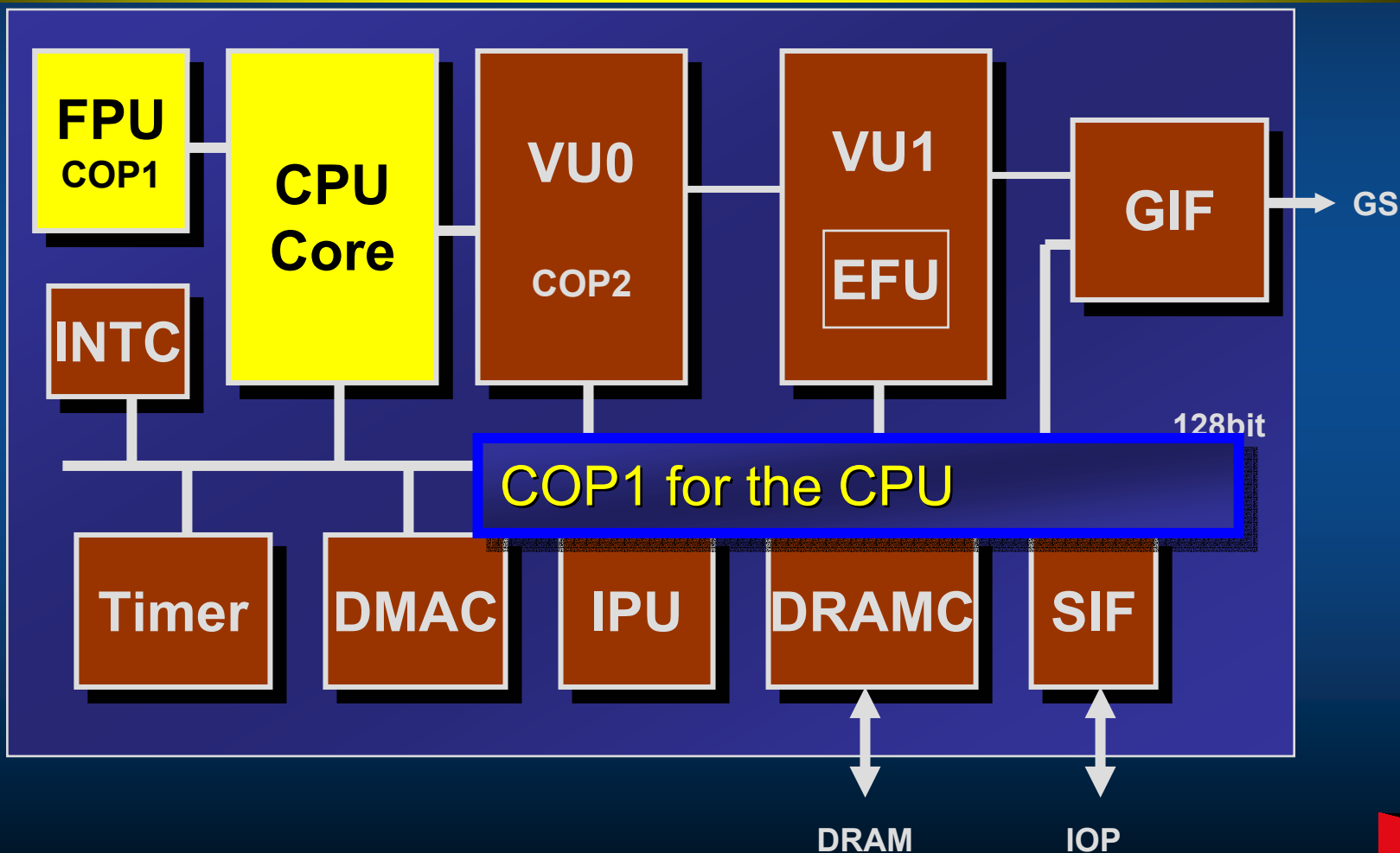
Emotion Engine architecture

CPU Core



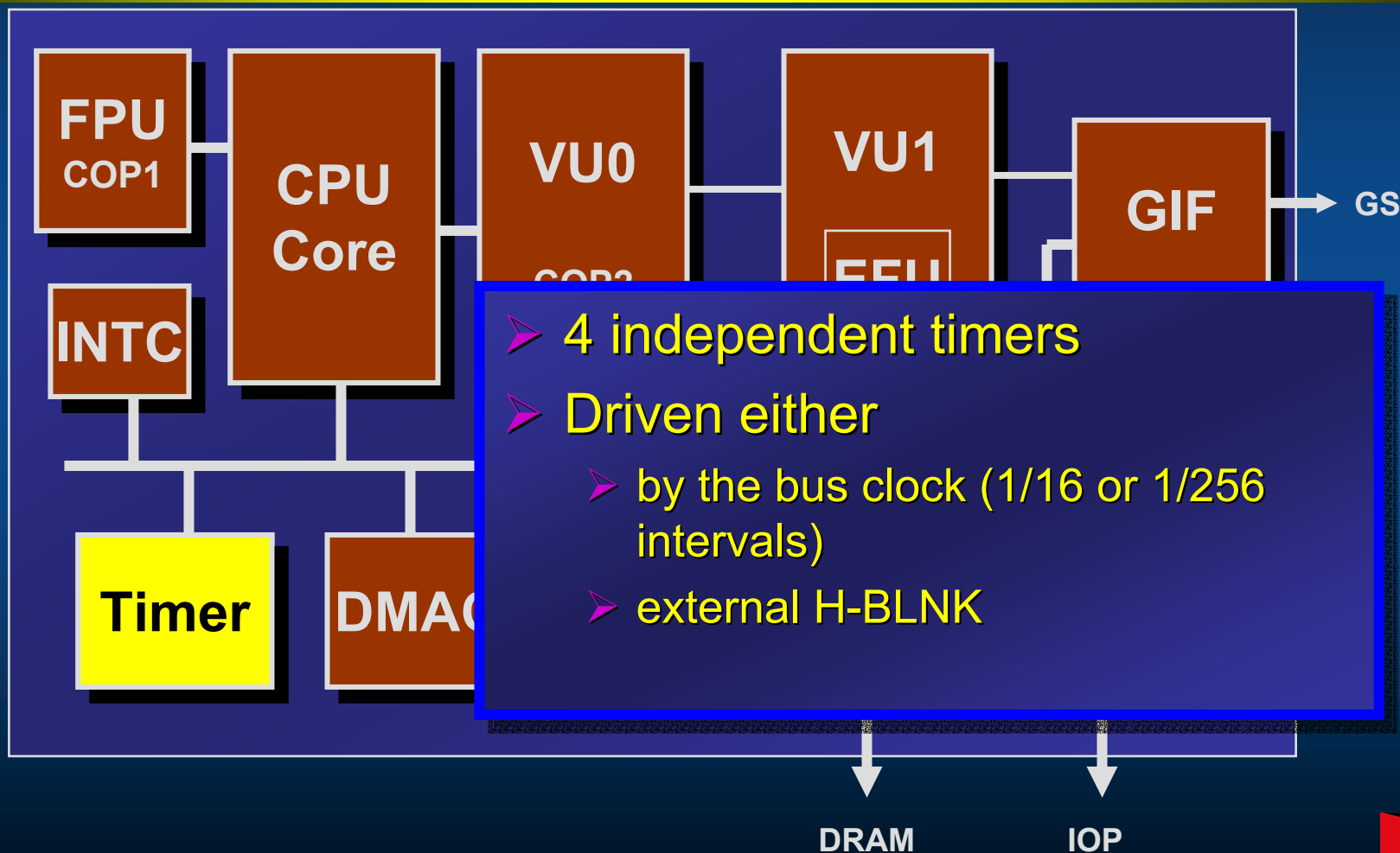
Emotion Engine architecture

Floating Point Unit (FPU)



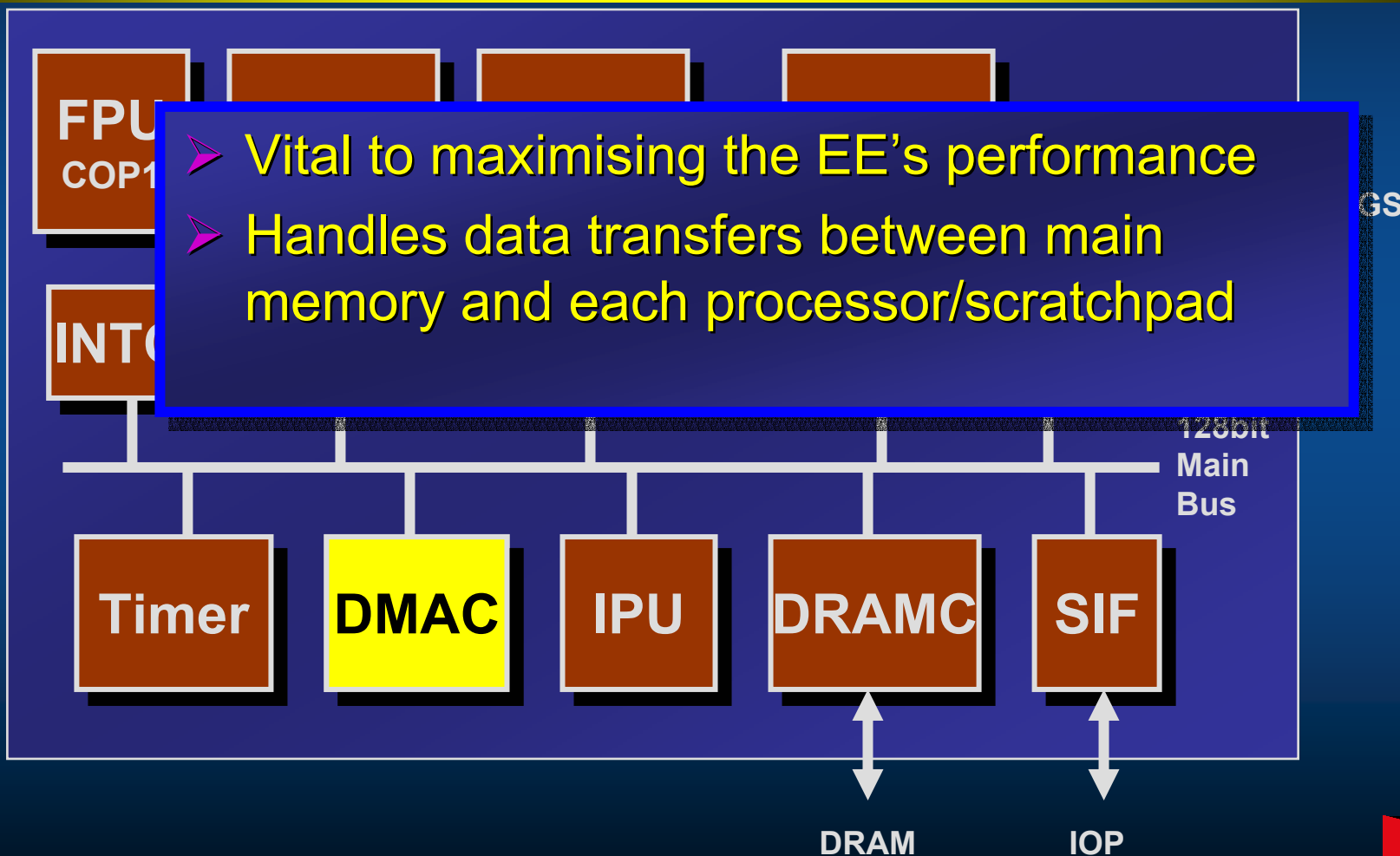
Emotion Engine architecture

Timer



Emotion Engine architecture

DMA Controller (DMAC)

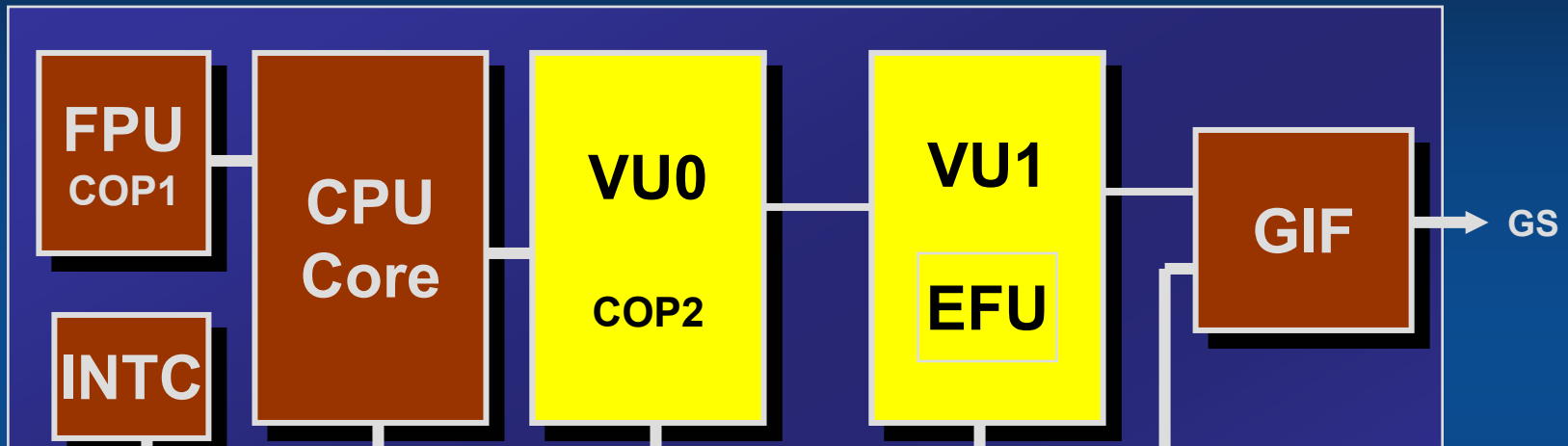


GS



Emotion Engine architecture

Vector Units (VU0 & VU1)

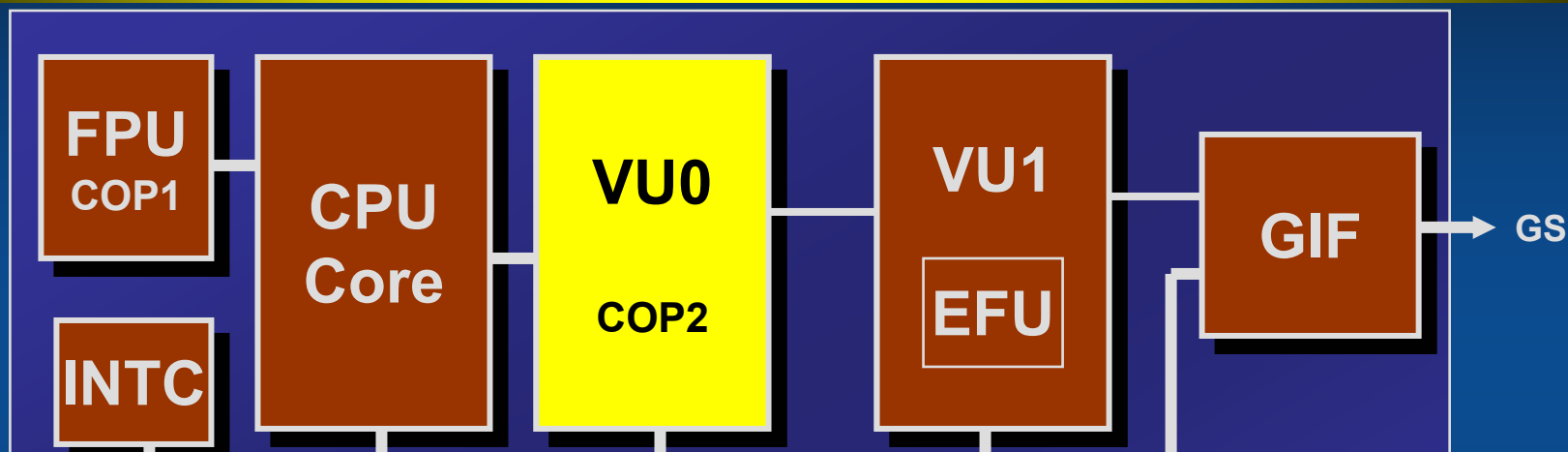


- Used for mathematical operations
- FMACs for addition and multiplication
- FDIV for division and square root operations
- Built-in memory for microprograms
- VIFs link the VUs to the rest of the system



Emotion Engine architecture

Vector Unit 0 (VU0)

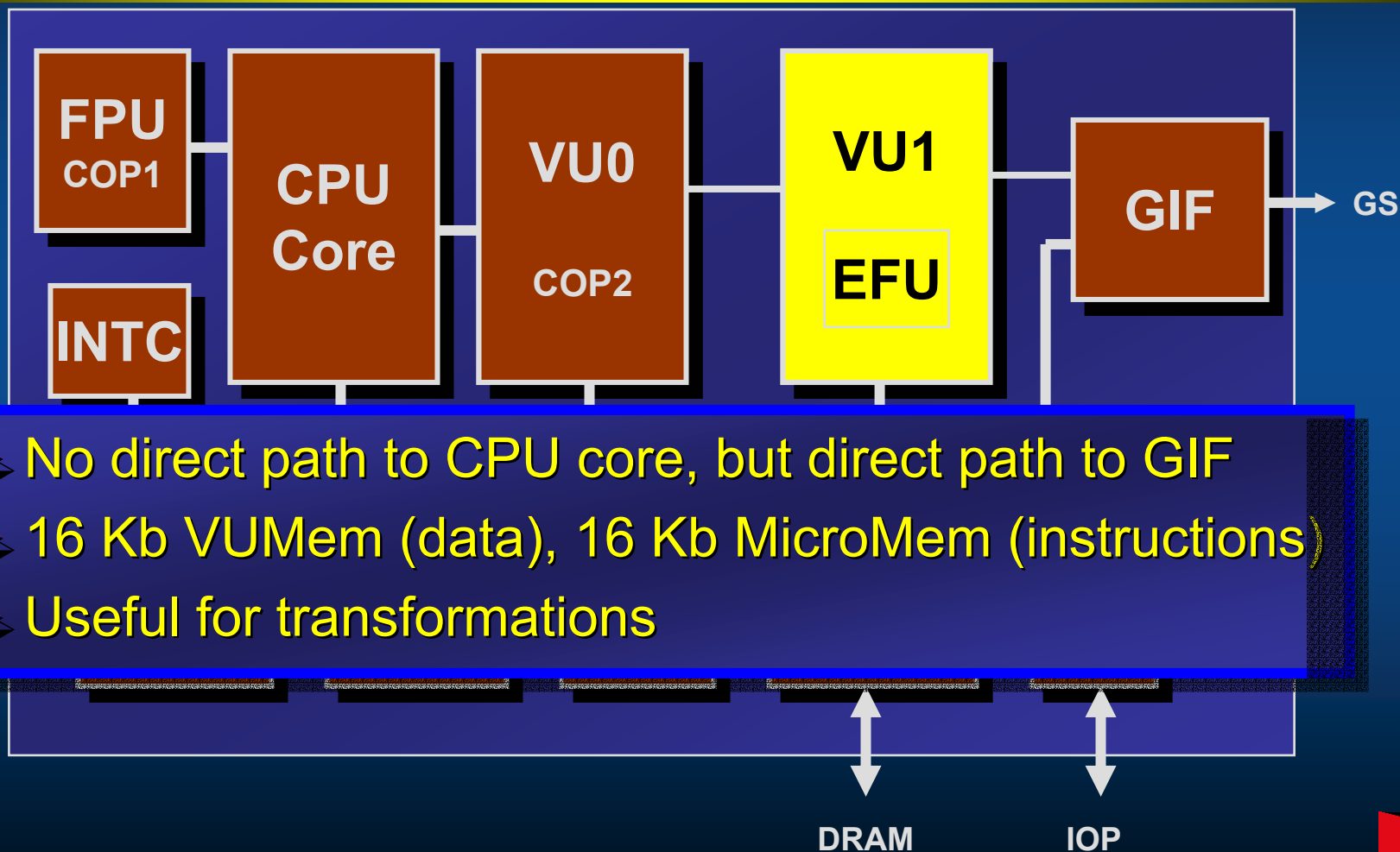


- 4 FMACs, 1 FDIV
- COP2 for the CPU, executing macroinstructions
- 4 Kb VUMem (data), 4 Kb MicroMem (instructions)
- Useful for complex operations like physics etc.



Emotion Engine architecture

Vector Unit 1 (VU1)



- No direct path to CPU core, but direct path to GIF
- 16 Kb VUMem (data), 16 Kb MicroMem (instructions)
- Useful for transformations



Emotion Engine architecture

Image Processing Unit (IPU)

- Image data decompression processor
- Decodes MPEG2 streams
- MacroBlock Decode
- Vector Quantization
- Transparency Control

GS

Timer

DMAC

IPU

DRAMC

SIF

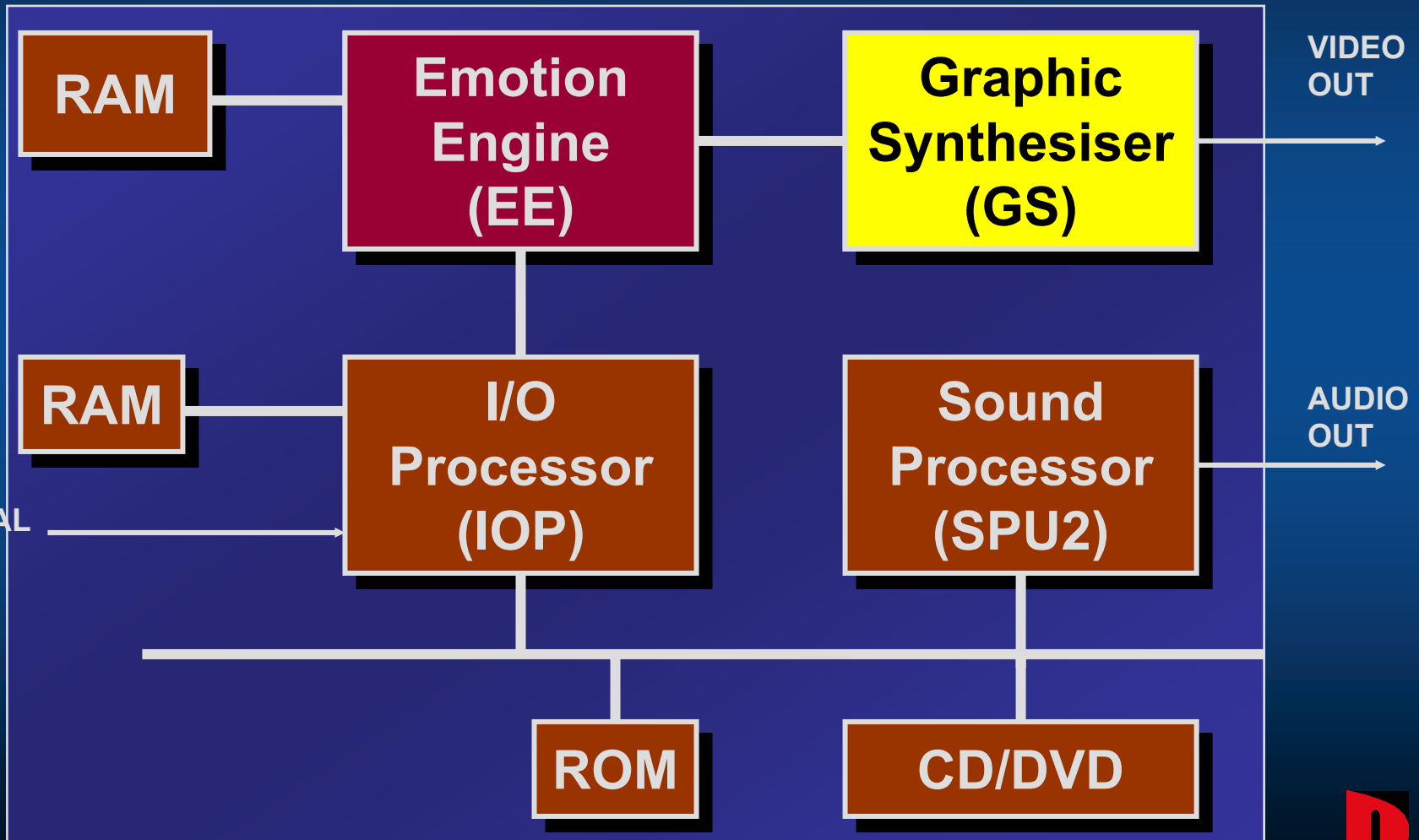
Bus

DRAM

IOP



System Architecture

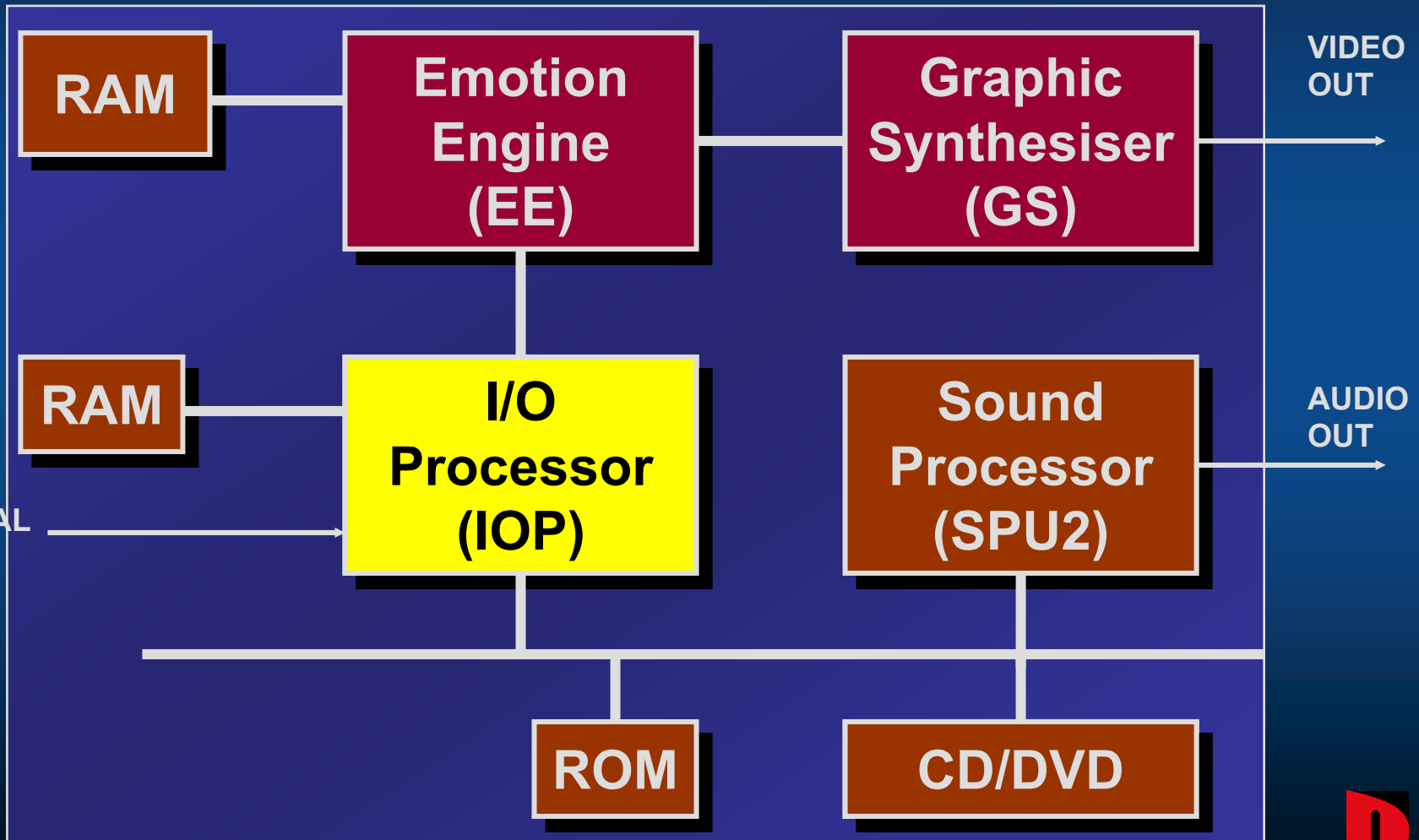


GS specifications

- Clock Frequency 150 Mhz
- Embedded DRAM 4MB
- Total memory bandwidth 1.2Gb/sec
- Pixel fill rate 2.4GPixel/sec



System Architecture

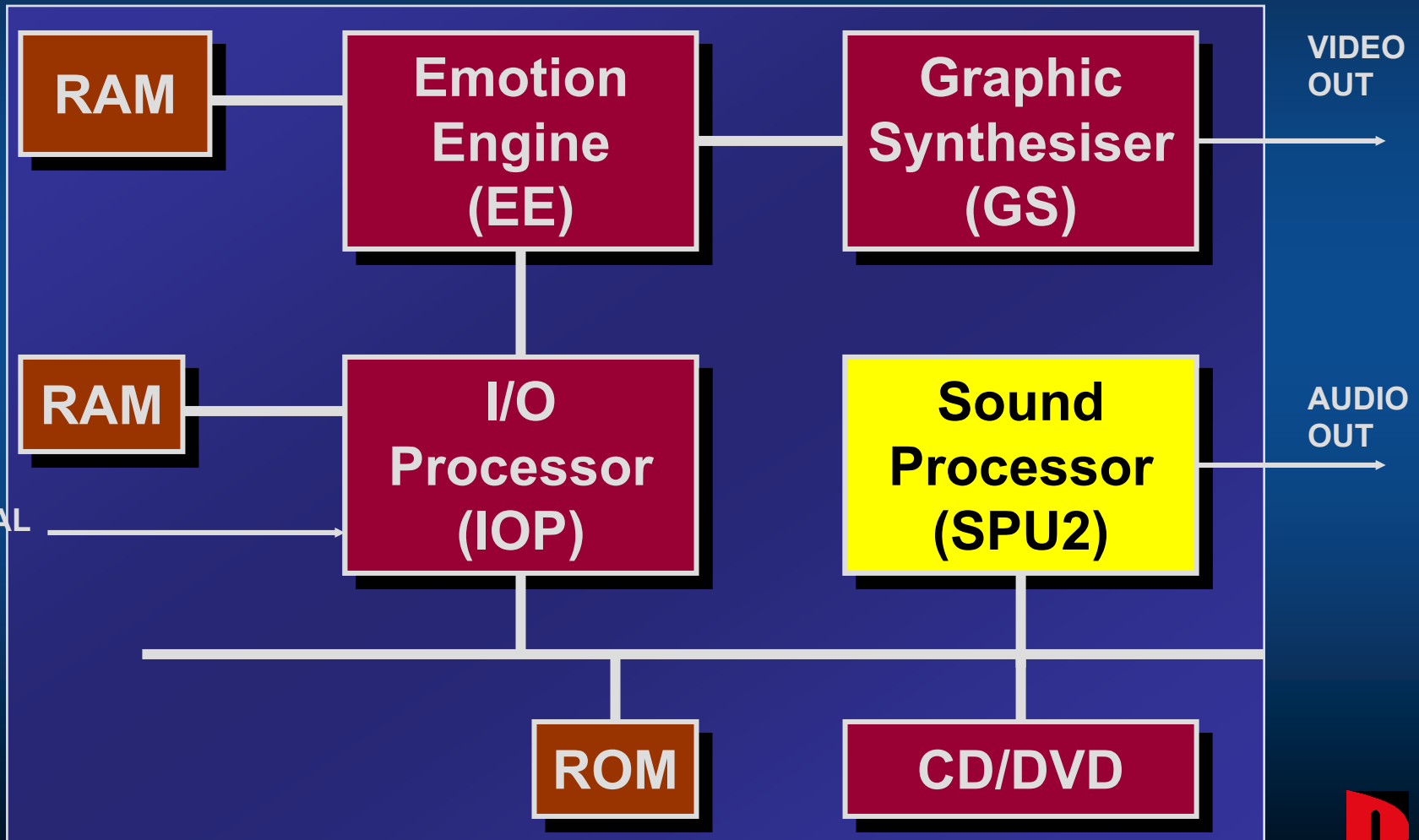


IOP

- Contains an R3000 (PlayStation CPU+)
- 2 clock frequencies
- 2 Mb IOP memory
- Interfaces to the EE for
 - controllers
 - memory devices
 - SPU 2
 - CD/DVD unit
 - USB/IEEE1394



System Architecture



SPU 2

- 2 DSP cores, 48 Channels
- 2Mb sound memory
- Output to DAC or Optical digital output



Standard Peripherals

- PS one peripherals compatible (most)
- “DualShock2” as standard controller
- Large capacity “memory card” (8Mb)
- USB and i.Link (aka IEEE 1394) devices (non proprietary interfaces)
- “broadband unit” (40GB HDD and network adaptor)



USB Applications

- Digital Camera (e.g. via “Picture Paradise” software or “eyetoy” game)
- Microphone (e.g. speech recognition and communication software in “SOCOM: US Navy Seals”)
- Scanner, Printer (Japan titles)
- Keyboards, Mouse (Yabasic, PS2 Linux)



And what happens next ...



Products based upon the “Cell Processor”

- A chip triumvirate of IBM, Sony and Toshiba has pledged \$400 million to the project and sent engineers to a joint development centre in Austin, Texas
- “We are working for the third-generation (PlayStation) with this very aggressive and crazy goal... Moore's Law is too slow for us.”
Shin'ichi Okamoto (SCE CTO)



Questions?

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